TECHNICAL MANUAL

AM-320

LINE PRINTER INTERFACE

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SECTION I
GENERAL DESCRIPTION

1.0 INTRODUCTION.

This manual provides operating and maintenance instructions for the AM-320 Line Printer Interface circuit board manufactured by Alpha Microsystems Inc., located in Irvine, California. Circuit board description, operating and usage instructions, programming, theory of operation, and maintenance instructions are included to provide the user with the information necessary to utilize this circuit board to its full capability.

1.1 CIRCUIT BOARD DESCRIPTION.

The AM-320 circuit board provides control and interface capability between an S-100 Bus system and Dataproducts interface line printers. The AM-320 operates as a buffered parallel port with 4K bytes of static RAM to allow full speed operation with minimum processor overhead. The write port accepts byte data and retains it until it can be written into buffer memory, and the read ports provide character count information. The data is then stored in buffer memory until it is accessed by the line printer.

1.2 APPLICATION.

This circuit board operates in S-100 Bus systems with either 8 or 16 bit format and requires no interrupt line. Interface control circuitry is provided for control of a line printer with either long line (differential lines) or short line (single lines) Dataproducts interface. For simplified block diagram see figure 1-1. See Section II of this manual for wiring instructions and system interface information. For complete information on the line printer, see the line printer maintenance manual.

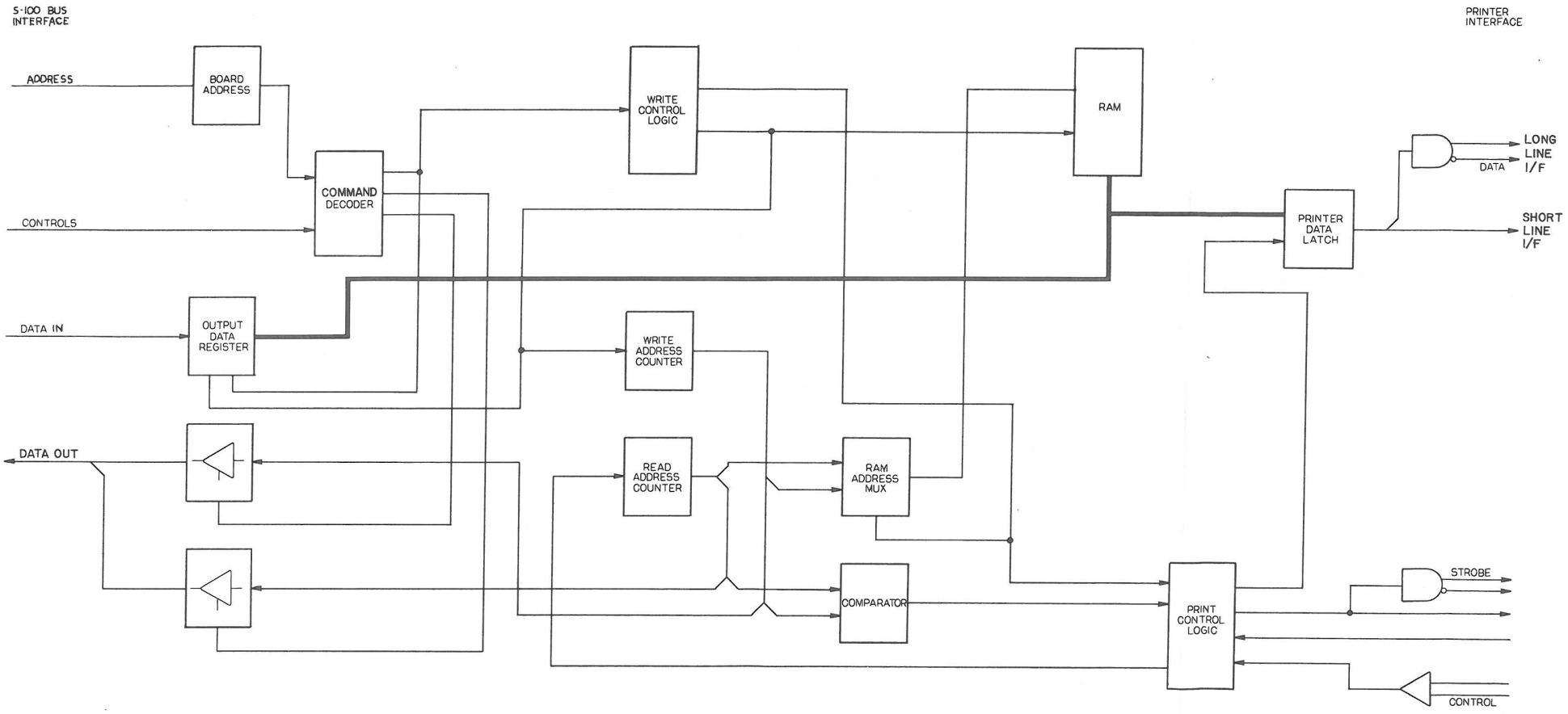


Figure 1-1.
AM-320 Line Printer Interface
Simplified Block Diagram.

SECTION II
OPERATING DATA

2.0 INTRODUCTION.

This section contains information on the use of the AM-320 line printer interface circuit board. Capabilities, specifications, interface wiring, and user option descriptions are provided for the successful integration of the AM-320 into the user's system.

2.1 CAPABILITIES AND SPECIFICATIONS.

This circuit board operates from the standard S-100 Bus structure to interface with Dataproducts interface line printers. Circuit board design accommodates either 8 or 16 bit S-100 Bus systems to interface with a single line printer. Detailed specifications are contained in Table 2-1.

Table 2-1. AM-320 Specifications

PARAMETER	SPECIFICATION
CPU Interface	Standard S-100 Bus, 8 or 16 bit.
Printers per Circuit Board	One
Drive Speeds	200, 300, 600, 900, 1100 and 1200 lines per minute matrix or band printers on Dataproducts interface.
Interrupts	None required.
Buffer	4K bytes of static buffer RAM to allow full speed operation with minimum processor overhead.
Printer Interface	Accepts long or short line Dataproducts interface.
Input Power	+8VDC @ 1.2A
Environment (operating) Circuit Board Temperature	60°F to 90°F (16°C to 32°C)
Humidity	10% to 80% (non-condensing)
Printer	See technical manual on individual printer.
Dimensions	5 1/4" x 10" (13.3 cm x 25.4 cm)

2.2 INSTALLATION AND START-UP.

When the AM-320 circuit board is received, it is ready for use. No adjustment or calibration is required for operation. The hardware requirements for installation and use are described in this section and the software requirements are described in Section III. Installation requirements for the line printer are contained in the line printer manual.

2.2.1 Installation.

First ensure that the proper power wiring is available and that the correct voltages are connected to the line printer and to the various pins of the circuit board as shown in Table 2-2. Line printer unpacking and mounting instructions are covered in the printer manual. The AC power requirements, line voltage options and fuse selection proedures are also described in the line printer manual.

Install the AM-320 circuit board into any available slot in the CPU chassis. Install the cable to the printer for either short or long line interface as follows:

a. For short line interface, connect the cable to J2 of the AM-320 circuit board. Match pin 1 of the cable (brown) to pin 1 of the connector. Connect the other end of the cable to the printer.

b. For long line interface, connect the cable to J3 of the AM-320 circuit board. Match pin 1 of the cable (brown) to pin 1 of the connector (arrow). Connect the other end of the cable to the printer.

See paragraph 2.4.3 of this manual for selection of short or long line options on the AM-320 circuit board.

2.2.2 System Start-up.

Set up the line printer spooler on the system as described in DWM-00100-38. Turn on system power and turn on the printer. Set up the line printer spooler by modifying the SYSTEM.INI and PRINTER INI. files as described in Section 2.7 of DWM-00100-19. Type on the terminal PRINT DSKO:SYSTEM.INI[1,4], CARRIAGE RETURN. The line printer will print the ontents of this file.

2.3 Interface Description.

The AM-320 line printer circuit board provides interface capability between the standard S-100 Bus structure and Dataproducts interface line printers. Both 8 and 16 bit S-100 Bus systems are compatible with the AM-320.

2.3.1 S-100 Bus Interface.

The AM-320 circuit board is fully S-100 Bus compatible. The board and its associated printer are addressed through the standard data lines and is compatible with either 8 or 16 bit S-100 Bus systems. The S-100 Bus connections are made via the bottom edge connector and are listed in Table 2-2. For a complete description of these signals and their operation in the AM-320, see Section IV of this manual.

2.3.2 Line Printer Interface.

The line printer utilizes an ASCII bit-parallel interface. The interface contains seven data lines, status lines, the demand line and the character strobe line. Interface levels are undefined during power ON and power OFF phases. After the printer has been placed ON LINE, the DEMAND line requests sequential data characters and a control character. The DEMAND line continues requesting characters until a control character is detected. Printer interface signals are listed in Table 2-3. For a complete description of these signals and their operation in the AM-320, see Section IV of this manual.

Table 2-2. Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
+7.5V	+ 7.5vdc Power	1
+16V	+ 16vdc Power	2
$\overline{\text{VI8}}$	Vectored Interrupt 8	3
$\overline{\text{VI0}}$	Vectored Interrupt 0	4
$\overline{\text{VI1}}$	Vectored Interrupt 1	5
$\overline{\text{VI2}}$	Vectored Interrupt 2	6
$\overline{\text{VI3}}$	Vectored Interrupt 3	7
$\overline{\text{VI4}}$	Vectored Interrupt 4	8
$\overline{\text{VI5}}$	Vectored Interrupt 5	9
$\overline{\text{VI6}}$	Vectored Interrupt 6	10
$\overline{\text{VI7}}$	Vectored Interrupt 7	11
RTC	Real Time Clock, 50Hz or 60Hz	12
POWFAIL	AC Power Failure Status	13
$\overline{\text{VI9}}$	Vectored Interrupt 9	14
A18	Address 18	15
A16	Address 16	16
A17	Address 17	17
$\overline{\text{STATDSB}}$	Status Disable	18
$\overline{\text{C/CDSB}}$	Command/Control Disable	19
GND	Ground	20

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
$\overline{\text{IODIS}}$	I/O Disable	21
$\overline{\text{ADDDSB}}$	Address Disable	22
$\overline{\text{DODSB}}$	Data Bus Disable	23
Ø2	Phase 2 Clock	24
$\overline{\text{STVAL}}$	Status and Address Valid	25
PHLDA	DMA Request Acknowledge	26
PWAIT	Processor Wait	27
N/U	Not Used	28
A5	Address 5	29
A4	Address 4	30
A3	Address 3	31
A15	Address 15	32
A12	Address 12	33
A9	Address 9	34
DOUT 1/D1	Data Bus Bit 1	35
DOUT 0/D0	Data Bus Bit 0	36
A10	Address 10	37

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
DOUT 4/D4	Data Bus Bit 4	38
DOUT 5/D5	Data Bus Bit 5	39
DOUT 6/D6	Data Bus Bit 6	40
DIN 2/D10	Data Bus Bit 10	41
DIN 3/D11	Data Bus Bit 11	42
DIN 7/D15	Data Bus Bit 15	43
SMI	Bus Master OP Code Fetch	44
SOUT	I/O Output Cycle	45
SINP	I/O Input Cycle	46
SMEMR	Memory Read Cycle	47
SHLTA	HLT Acknowledge	48
$\overline{\text{PERR}}$	Parity Error Pulse	49
GND	Ground	50
+7.5V	+7.5vdc Power	51
-16V	-16vdc Power	52
GND	Ground	53
$\overline{\text{SLAVECLR}}$	Reset Signal To All I/O Devices	54

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
$\overline{\text{DMA0}}$	DMA Controller Arbitration	55
$\overline{\text{DMA1}}$	Lines For Use With Standard	56
$\overline{\text{DMA2}}$	S-100 Bus DMA System	57
$\overline{\text{SXTRQ}}$	16 Bit Cycle	58
A19	Address 19	59
N/U	Not Used	60
A20 A21 A22 A23	Address 20 Address 21 Address 22 Address 23	61 62 63 64
$\overline{\text{ADVAL}}$	Address Valid On Data Bus	65
$\overline{\text{WRDIS}}$	Write Disable	66
PHANTOM	ROM Memory Enable	67
N/U N/U	Not Used Not Used	68 69
Gnd	Ground	70
N/U	Not Used	71
PRDY	Processor Ready	72

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
N/U	Not Used	73
$\overline{\text{PHOLD}}$	DMA Request	74
$\overline{\text{PRESET}}$	Preset	75
PSYNC	Processor Sync, Start of Bus Cycle	76
$\overline{\text{PWR}}$	Write Strobe	77
PDBIN	Data Bus Input Command	78
A0	Address 0	79
A1	Address 1	80
A2	Address 2	81
A6	Address 6	82
A7	Address 7	83
A8	Address 8	84
A13	Address 13	85
A14	Address 14	86
A11	Address 11	87
DOUT 2/D2	Data Bus Bit 2	88
DOUT 3/D3	Data Bus Bit 3	89
DOUT 7/D7	Data Bus Bit 7	90
DIN 4/D12	Data Bus Bit 7	91
DIN 5/D13	Data Bus Bit 13	92
DIN 6/D14	Data Bus Bit 14	93
DIN 1/D9	Data Bus Bit 9	94
DIN 0/D8	Data Bus Bit 8	95

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
SINTA	Interrupt Acknowledge	96
$\overline{\text{SWO}}$	Bus Master Output	97
$\overline{\text{ERROR}}$	Memory Error Interrupt	98
$\overline{\text{BERR}}$	Bus Error	99
GND	Ground	100

Table 2-3. Line Printer Interface Signals List

PIN	SIGNAL	AM-320 IN/OUT	PIN	SIGNAL	AM-320 IN/OUT
J2-1	STROBE	OUT	J3-1	STROBE +	OUT.
J2-2	GND		J3-2	STROBE -	
J2-3	Data 7	OUT	J3-3	Data 7 +	OUT
J2-4	GND		J3-4	Data 7 -	
J2-5	Data 6	OUT	J3-5	Data 6 +	OUT
J2-6	GND		J3-6	Data 6 -	
J2-7	Data 5	OUT	J3-7	Data 5 +	OUT
J2-8	GND		J3-8	Data 5 -	
J2-9	Data 4	OUT	J3-9	Data 4 +	OUT
J2-10	GND		J3-10	Data 4 -	
J2-11	Data 3	OUT	J3-11	Data 3 +	OUT
J2-12	GND		J3-12	Data 3 -	
J2-13	Data 2	OUT	J3-13	Data 2 +	OUT
J2-14	GND		J3-14	Data 2 -	
J2-15	Data 1	OUT	J3-15	Data 1 +	OUT
J2-16	GND		J3-16	Data 1 -	
J2-17	Data 0	OUT	J3-17	Data 0 +	OUT
J2-18	GND		J3-18	Data 0 -	
J2-19	READY	IN	J3-19	READY +	IN
J2-20	GND		J3-20	READY -	
J2-21	ON LINE	IN	J3-21	ON LINE	IN
J2-22	GND		J3-22	ON LINE -	
J2-23	DEMAND	IN	J3-23	DEMAND	IN
J2-24	GND		J3-24	DEMAND -	

2.4 USER OPTIONS.

Some features of the AM-320 can be changed by selection of jumpers and IC's at the user's option. Location of jumper pads is shown in Figure 2-1.

2.4.1 Address Code.

Circuit board addressing can be selected at the user's option for any address block (in increments of four) on the address lines AD2-AD7. The standard address block is :C2-C3 (Hex) and is contained in etch when the circuit board is manufactured. To change the address, cut the desired etch and jumper for pull-up or ground to generate the desired board address.

2.4.2 Clock Selection.

The frequency of the circuit board clock generator is selectable for either 2 MHz or 1 MHz. For 2 MHz clock, the pads at CLK are jumpered. For 1 MHz clock, the pads at C/2 are jumpered. The standard clock is 2 MHz and is contained in etch.

2.4.3 Long Line - Short Line Select.

The AM-320 circuit board supports both long and short line Dataproducts interfacing. If long line interface is desired, U2 is removed (7414) and U4, U5 (8820), and U1, U3, U11, U12 and U13 (8830) are inserted. The interface cable must then be connected to J3. If short line interface is desired, U2 is inserted (7414), and U1, U3, U4, U5, U11, U12, and U13 are removed. The interface cable must then be connected to J2.

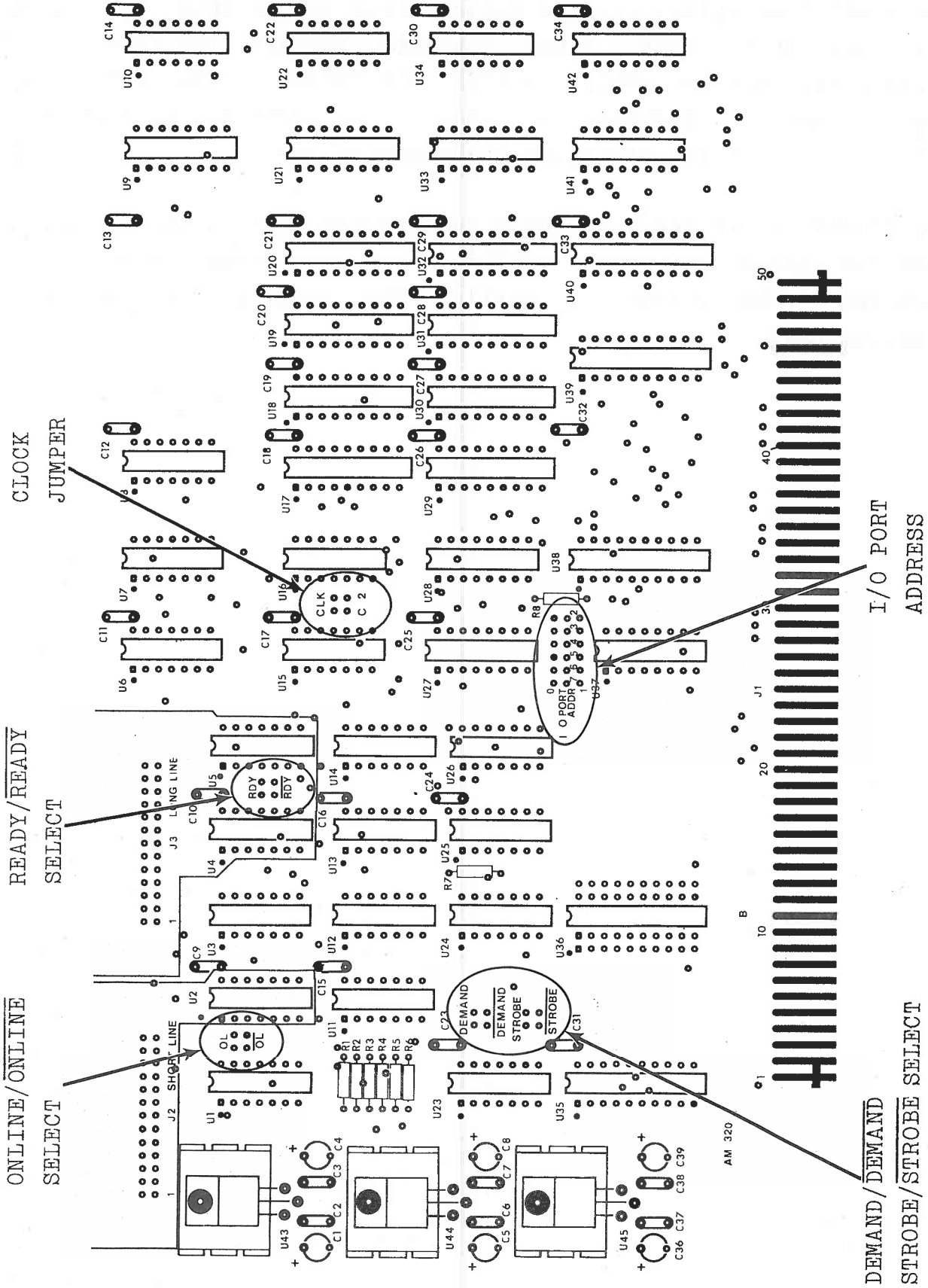


Figure 2-1. Location Of Jumpers For User Options

2.4.4 Line Printer Control Logic Signal Polarity Options.

For short line operation, the control line inputs from the printer may have their logic sense inverted (single line inputs). The signals involved are READY, ON LINE, and DEMAND. The active high input sense is strapped in etch. The logic may be reversed by cutting the etch and strapping the opposite pads.

The STROBE output logic may also be selected for both normal and inverted sense operation. The active high output is strapped in etch and can be reversed by cutting the etch and strapping the opposite pads.

SECTION III
PROGRAMMING

3.0 INTRODUCTION.

This section provides the programming requirements for the AM-320 circuit board. Read and write operations are described for complete system compatibility.

3.1 I/O PORT DEFINITIONS.

Two I/O ports are required by the line printer interface:

BOARD ADDR	WRITE	READ
C2:	DATA	LINE PRINTER OUTPUT CHARACTER COUNT
C3:	RESET	AM-100 INPUT CHARACTER COUNT

3.2 DATA TRANSFER OPERATIONS.

The AM-320 circuit board is basically a buffered parallel port. The WRITE port at the base address accepts byte data and retains it until it can be written into buffer memory. The WRITE port at base address +1, or port C3 (hex) is used to reset the AM-320 through software control.

Two status READ ports are provided that supply a character count. The base port count is the count of the number of characters accepted by the printer divided by 16. The next port's count is the number of characters supplied to the interface board by the processor divided by 16. For highest speed performance, data should be transferred to the interface until the processor character count is one less than the printer character count. When the interface is next serviced, this situation should again be established. In this way, the buffer of 4096 characters will be used to its maximum effectiveness. Should the processor be unable to service the interface for a period of time, printer speed will be unimpaired.

SECTION IV
FUNCTIONAL THEORY OF OPERATION

4.0 INTRODUCTION.

The AM-320 Line Printer Interface circuit board contains integrated circuit elements for the data processing necessary for the performance of the functions described in Sections I, II and III of this manual. This section describes the functional theory of operation of the circuit board and also provides information for each of the integrated circuit elements.

4.1 CIRCUIT BOARD OPERATION.

This circuit board provides control and interface capability between the S-100 Bus and Dataproducts interface line printers. The functional block diagram of the circuit board is shown in Figure 4-1. The circuit board schematic, parts list, and component cross reference list are contained in Section VI of this manual. Table 4-1 contains a list of the signals used in the circuit board with descriptions of their functions. For S-100 Bus interface signals, see Table 4-2. For line printer interface signals, see Table 4-3.

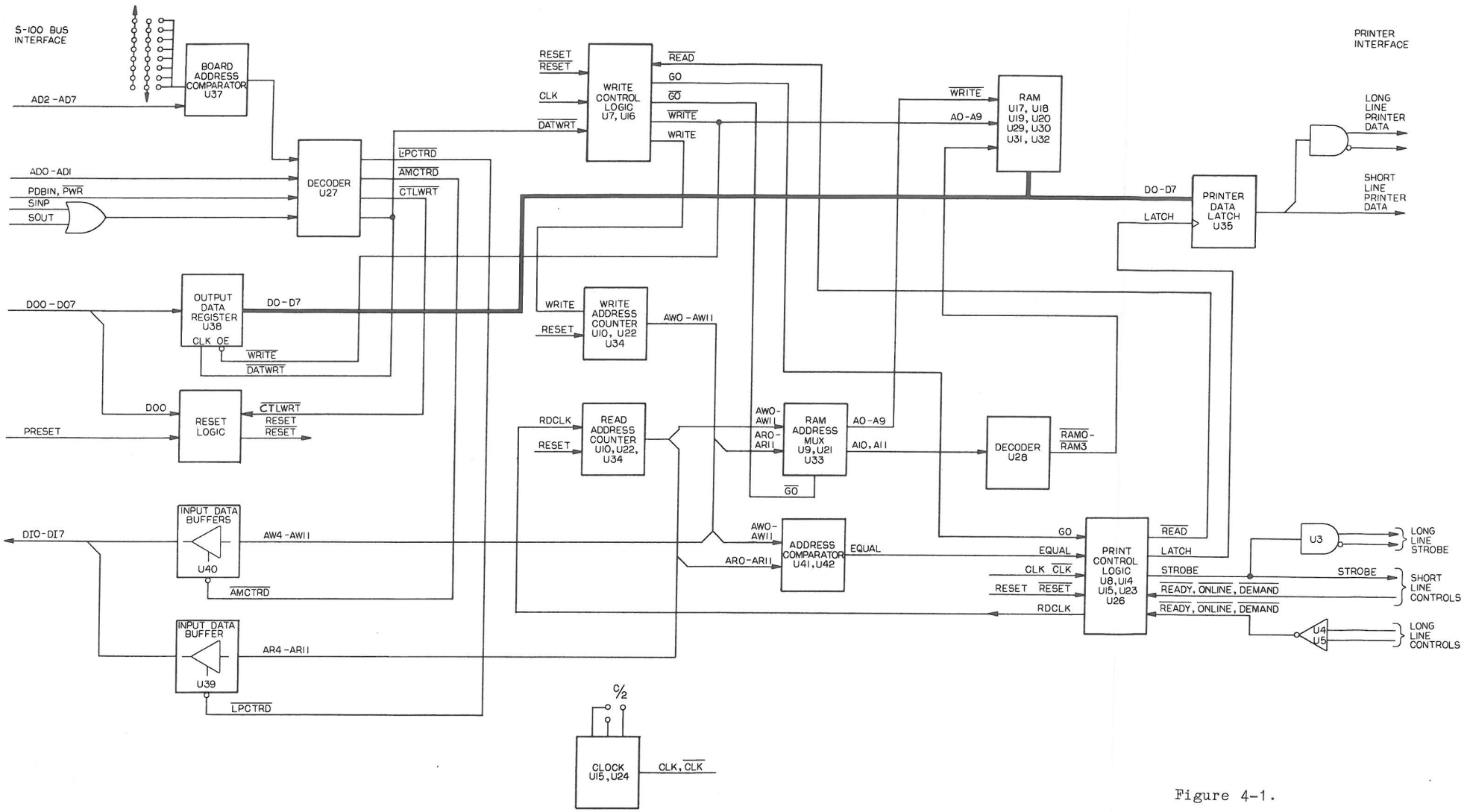


Figure 4-1.
AM-320 Line Printer Interface
Functional Block Diagram

Table 4-1. AM-320 Signal Descriptions

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
A0-A9	RAM Address Bus	1	RAM address lines from the multiplexer that selects either the read address or write address.
$\overline{\text{AMCTRD}}$	AM-100 Count Read	1	Gates the contents of the write address counter on to the data input line DI0-DI7.
AR0-AR11	Read Address	2	RAM read address generated by the read address counter.
AW0-AW11	Write Address	1	RAM write address generated by the write address counter.
CLK $\overline{\text{CLK}}$	Clock	1	Circuit board clock.
$\overline{\text{CTLWRT}}$	Control Write	1	Decoder output to reset the AM-320 with data bit D0.

Table 4-1. (Con't) AM-320 Signal Descriptions

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
DATWRT	Data Write	1	Output of the decoder for a processor write operation. Clocks processor data into the output data register and initiates the write control logic.
D0-D7	Data Bus Bits 0-7	1,2	Internal tri-state data bus between the internal memory, processor data port, and printer output port.
EQUAL	Address Equal	2	Asserted when read address AR0-AR11 is equal to write address AW0-AW11.
GO $\overline{GO}$	Go	1	Asserted during a write operation by VALID to generate WRITE and select AW0-AW11 for RAM addressing.
LATCH	Printer Data Latch	2	Latches data from memory into the printer data latch for a printer read operation. Asserted when GO, EQUAL, and STROBE are all low and printer $\overline{READY}$, $\overline{ON\ LINE}$, and $\overline{DEMAND}$ are low.

Table 4-1. (Con't) AM-320 Signal Descriptions

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
LPCTRD	Line Printer Count Read	1	Gates the contents of the read address counter on to the data input lines DI0-DI7.
$\overline{\text{RAM0}}$ $\overline{\text{RAM3}}$	RAM Select	1	Selects the desired RAM. Generated from RAM address bits A10 and A11.
RDCLK	Read Clock	2	Generated during a printer read operation by LATCH and CLK to advance the read address counter.
$\overline{\text{READ}}$	Printer Read	2	Asserted during a printer read operation. Generated when printer $\overline{\text{READY}}$, $\overline{\text{ON LINE}}$, and $\overline{\text{DEMAND}}$ are low, and GO, EQUAL, and STROBE are all low. Generates STROBE on the next clock.
RESET $\overline{\text{RESET}}$	Reset	1	Circuit board reset signal generated from S-100 Bus PRESET or from CTLWRT and D00.

Table 4-1. (Con't) AM-320 Signal Descriptions

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
VALID	Data Valid	1	Asserted during a processor write operation by DATWRT to generate signal GO.
WRITE $\overline{\text{WRITE}}$	Processor Write	1	Asserted during a processor write operation by GO to enable a write to the RAM, i.e., enable the data in the output data register onto the data bus DO-D7, and advance the write address counter.

Table 4-2. S-100 Bus Interface Signal Descriptions

MNEMONIC	NAME	PIN	DESCRIPTION
AD0	Address 0	79	8 bits of S-100 addressing.
AD1	Address 1	80	
AD2	Address 2	81	
AD3	Address 3	31	
AD4	Address 4	30	
AD5	Address 5	29	
AD6	Address 6	82	
AD7	Address 7	83	
DI0	Input Data Bit 0	95	Data input port. Bus master input from slaves.
DI1	Input Data Bit 1	94	
DI2	Input Data Bit 2	41	
DI3	Input Data Bit 3	42	
DI4	Input Data Bit 4	91	
DI5	Input Data Bit 5	92	
DI6	Input Data Bit 6	93	
DI7	Input Data Bit 7	43	
DO0	Output Data Bit 0	36	Data output port. Bus master output to slaves.
DO1	Output Data Bit 1	35	
DO2	Output Data Bit 2	88	
DO3	Output Data Bit 3	89	
DO4	Output Data Bit 4	38	
DO5	Output Data Bit 5	39	
DO6	Output Data Bit 6	40	
DO7	Output Data Bit 7	90	
PDBIN	Data Bus In	78	Read enable. Used by bus master to request addressed slave to place data on input port.

Table 4-2. (Con't) S-100 Bus Interface Signal Descriptions

MNEMONIC	NAME	PIN	DESCRIPTION
$\overline{\text{PWR}}$	Write Strobe	77	Write strobe generated by bus masters as write command to slaves.
$\overline{\text{PRESET}}$	Reset	75	AM-320 reset input from bus.
SINP	I/O Input Cycle	46	AM-320 I/O signal indicating I/O input operation.
SOUT	I/O Output Cycle	45	AM-320 I/O signal indicating I/O output operation.
+8VDC	+8VDC	1, 51	+8V power.
GND	Ground	50, 100	System Ground.

Table 4-3. Line Printer Interface Signal Description.

SIGNAL	J2 PIN	J3 PIN	DESCRIPTION
Data 0	17	+ 17	Data lines to the printer to carry the codes for the character set as well as the control codes. Data must be stable on the lines for 50 ns prior to and after the generation of STROBE.
	Gnd 18	- 18	
Data 1	15	+ 15	
	Gnd 16	- 16	
Data 2	13	+ 13	
	Gnd 14	- 14	
Data 3	11	+ 11	
	Gnd 12	- 12	
Data 4	9	+ 9	
	Gnd 10	- 10	
Data 5	7	+ 7	
	Gnd 8	- 8	
Data 6	5	+ 5	
	Gnd 6	- 6	
Data 7	3	+ 3	
	Gnd 4	- 4	
DEMAND	23	+ 23	AM-320 input to synchronize data transfer. If the printer is ON LINE, the DEMAND line is asserted logical 1 to request a character from the AM-320. DEMAND remains high until STROBEA is received by the printer and then goes low.
	Gnd 24	- 24	

Table 4-3. (Con't) Line Printer Interface Signal Description.

SIGNAL	J2 PIN	J3 PIN	DESCRIPTION
ON LINE	21 Gnd 22	+ 21 - 22	AM-320 input to indicate that the printer has been placed on line. This signal is asserted when the printer ON LINE switch is activated and the printer is ready.
READY	19 Gnd 20	+ 19 - 20	AM-320 input that indicates that the printer is ready to be put ON LINE by the operator.
STROBE	1 Gnd 2	+ 1 - 2	AM-320 output that indicates that a data character has been placed on the data lines. When STROBE occurs, the printer samples the data lines and then brings DEMAND low while the character is being stored. See Figure 4-2 for timing.

The AM-320 consists of a random access memory (4K bytes), address counters, I/O registers, control logic, and the necessary drivers and receivers for line printer interface. Two connectors are provided on the top edge of the circuit board. One is for short line printer interface (J2), and the other is for long line printer interface (J3).

4.1.1 Circuit Board Reset.

The AM-320 may be reset by asserting S-100 Bus PRESET signal or by software control. A write to base address plus one or port C3 (hex) is used for circuit board reset. This generates signal $\overline{\text{CTLWRT}}$ which is ANDed with D00 to produce RESET.

4.1.2 Addressing.

Address data is received from S-100 Bus address lines AD0-AD7. Address lines AD2-AD7 are supplied to comparator U37 to produce a board select signal which is applied to decoder U27 along with AD0, AD1 and bus control signals PWR, PDBIN, SINP and SOUT. Decoder U27 generates the four signals for circuit board read and write operations.

4.1.3 CPU I/O Operations.

Two status read ports are provided by the AM-320. Buffers on U40 provide access to the eight highest order bits of the write address counter AW4-AW11, which contain the number of characters supplied to the AM-320 divided by 16. Buffers on U39 provide the eight highest order bits of the read address counter which contain the number of characters accepted by the printer divided by 16.

When the processor is writing data to the AM-320, $\overline{\text{DATWRT}}$ signal latches 8 bits of data into U38. This is 8 bits of low byte data regardless of whether the processor is 8 or 16 bits wide. Signal $\overline{\text{DATWRT}}$ then clocks U7 which presets VALID to high. If the printer is not reading data from the buffer memory, $\overline{\text{GO}}$ will be low on the next clock cycle. This activates the buffer memory write operation.

When $\overline{GO}$ is low, the address to the RAM is selected from the write address counter AWO-AW11 by RAM address MUX (U9, U21, U33). The rising edge of the next clock activates WRITE which enables the output data register U38. This applies the contents of U38 to the RAM via the data bus DO-D7. Signal $\overline{WRITE}$ also sets the RAM to the write mode and the data is written into the location selected by the write address counter AWO-AW11. The rising edge of WRITE clocks the write address counter to the next memory address.

4.1.4 Printer Read Operations.

After a processor write operation, the write address and the read address become unequal as detected by the address comparator (U41, U42). If GO, EQUAL and STROBE are all low, and printer signals $\overline{READY}$, $\overline{ON\ LINE}$ and $\overline{DEMAND}$ are asserted, a printer read operation activates. Since GO is inactive (low), GO is high which causes the RAM address MUX to select ARO-AR11 from the read address counter and $\overline{WRITE}$ is high which sets the RAM to the read state. The rising edge of $\overline{CLK}$ generates LATCH which latches the eight bits of data from the RAM into the printer data latch U35 via data bus DO-D7. The interfacing signal STROBE is generated from $\overline{READ}$ and $\overline{CLK}$ and is negated when DEMAND from the printer goes inactive. Figure 4-2 contains a timing diagram of the printer/AM-320 interface connector.

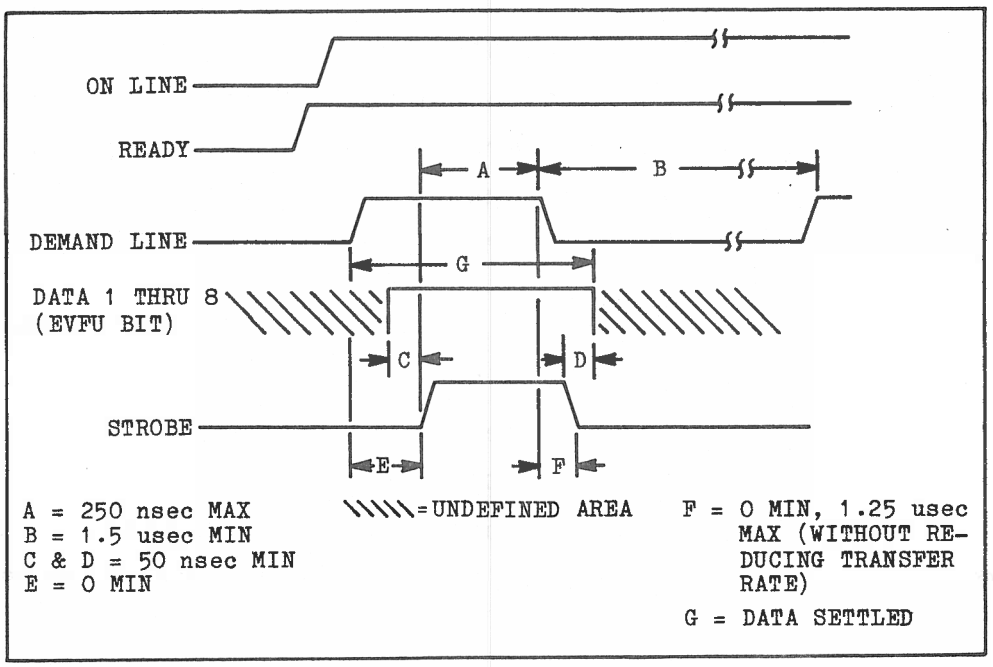


Figure 4-2. AM-320/Printer Interface Timing.

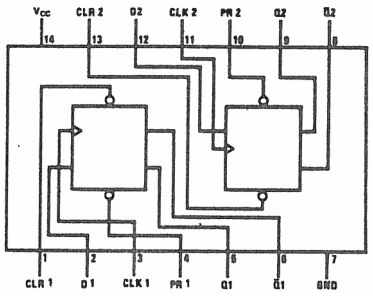
4.2 CIRCUIT MODULE DESCRIPTION.

This section describes the operation of the individual circuit modules (DIPS) contained on the AM-320 circuit board. Logic and connections are given with a brief description of module operation. Reference designators of the modules contained on the circuit board are given in the title of each paragraph. See Section VI for a complete cross reference list of the circuit modules and descriptive paragraphs.

4.2.1 Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear (U7, U15, U16).

For logic and connections, see Figure 4-3.

Connection Diagram



Truth Table

INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\bar{Q}$0

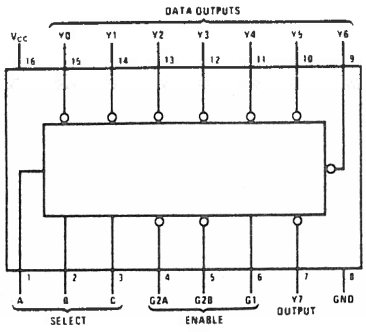
Notes: ⎍⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Figure 4-3. Dual D Flip-Flop Connections.

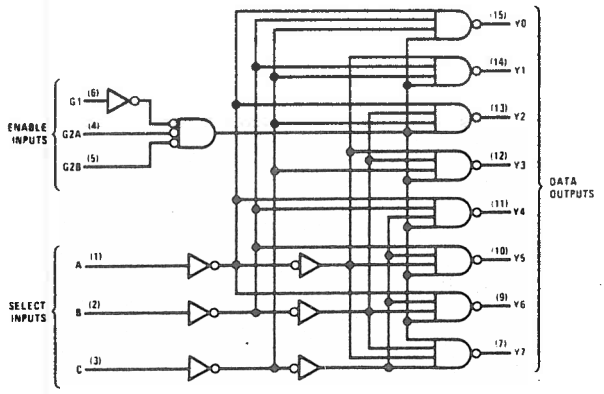
4.2.2 Decoder (U27).

These are Schottky-clamped circuits designed for memory-decoding or data-routing applications requiring very short propagation delay times. This DIP decodes one of eight lines based on the conditions at the three binary select inputs and the three enable inputs. For logic and connections, see Figure 4-4.

Connection Diagram



Logic Diagram



Truth Table

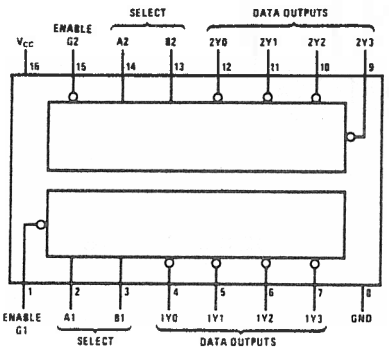
INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Figure 4-4. Decoder Connections.

4.2.3 Decoder/Demultiplexer (U28).

These Schottky-clamped circuits are designed to be used in high performance memory decoding or data routing applications requiring very short propagation delay times. This device contains two separate two-line to four-line decoders in one package. The active-low enable input can be used as a data line in demultiplexing applications. The device features fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high performance Schottky diodes to suppress line-ringing. For logic and connection, see Figure 4-5.

Connection Diagram



Logic Diagram

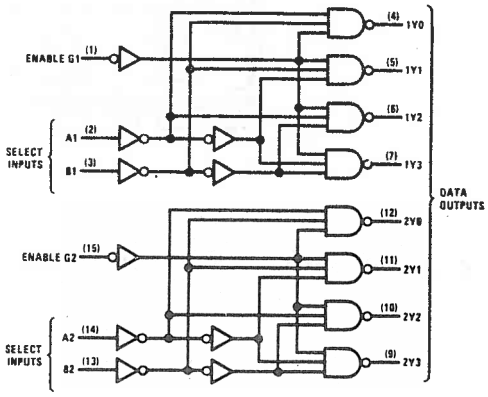


Figure 4-5. Decoder. Demultiplexer Connections.

4.2.4 Noninverting Octal Bus Driver (U39, U40).

These buffers provide the drive capability for tri-state bus requirements and are noninverting. For logic and connections, see Figure 4-6.

Connection Diagram

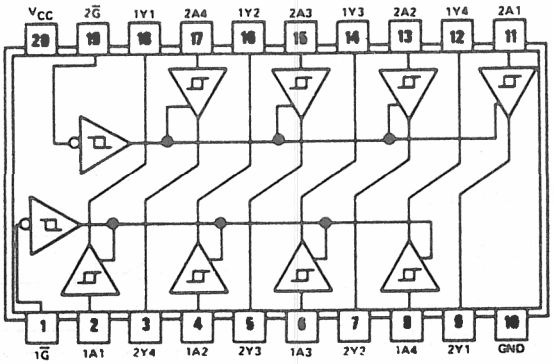
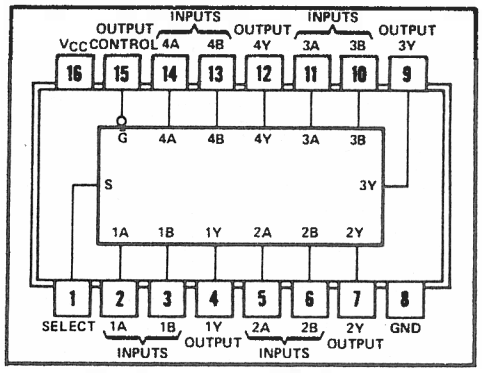


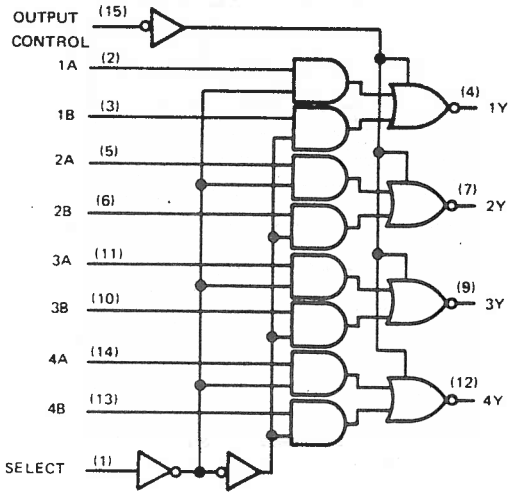
Figure 4-6. Noninverting Bus Driver Connections.

4.2.5 Tri-State Quad Two-Data Selectors/Multiplexers (U9, U21, U33). These multiplexers feature tri-state outputs that interface directly with data lines of bus systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possiblity that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times. For logic and connections, see Figure 4-7.

Connection Diagram



Logic Diagram



Truth Table

INPUTS				OUTPUT Y	
OUTPUT CONTROL	SELECT	A	B	'LS257A 'S257	'LS258A 'S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

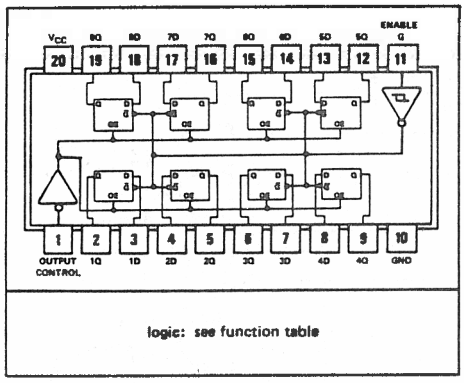
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

Figure 4-7. Two-Data Selectors/Multiplexer Connections

4.2.6 Octal D-Type Transparent Latch (U35).

This 8 bit register is a transparent D-type latch with three-state outputs. While the enable (G) is high, the Q outputs follow the data (D) inputs. When the enable is low, the output will be latched at the level of the data that was set up. For logic and connections, see Figure 4-8.

Connection Diagram



Truth Table

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Logic Diagram

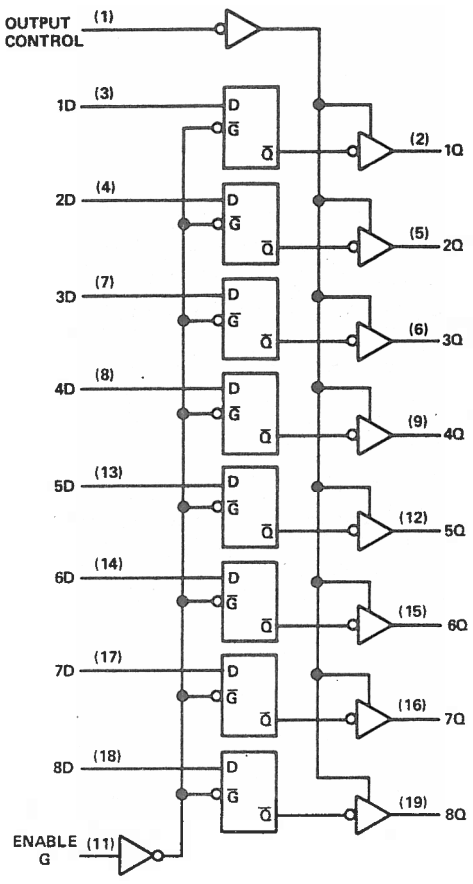
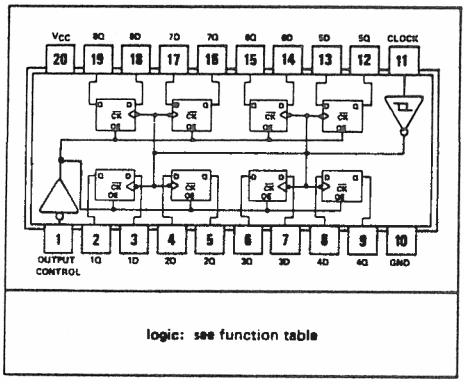


Figure 4-8. Transparent Latch Logic and Connections.

4.2.7 Tri-State D Flip-Flops (U38).

These 3 bit registers contain D-type flip-flops with totem-pole tri-state outputs capable of driving highly capacitve or low impedance loads. When the output control is taken to a high logic level, the outputs go into the high impedance state. When a low logic level is applied to the output control, data at the D inputs are loaded into their respective flip-flops on the next positive-going transition of the clock. For logic and connections, see Figure 4-9.

Connection Diagram



Truth Table

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Logic Diagram

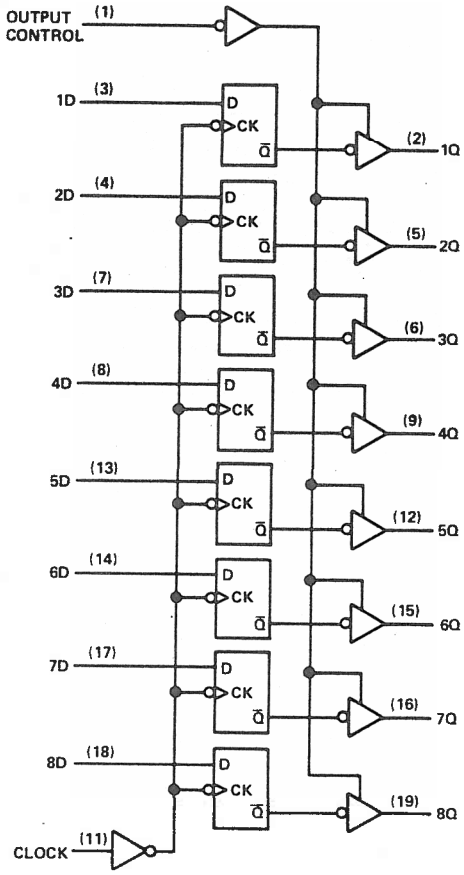
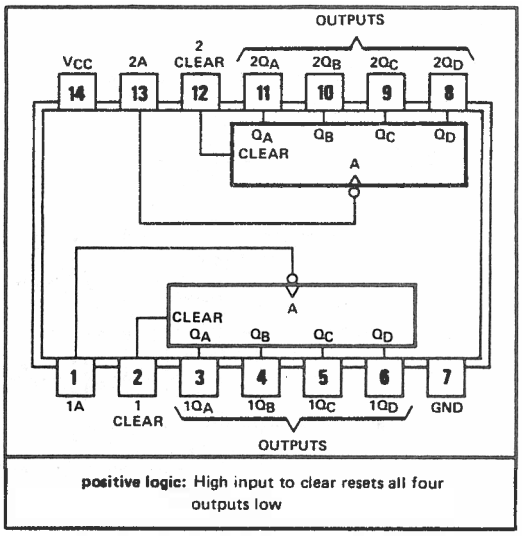


Figure 4-9. Tri-State D Flip-Flop Connections.

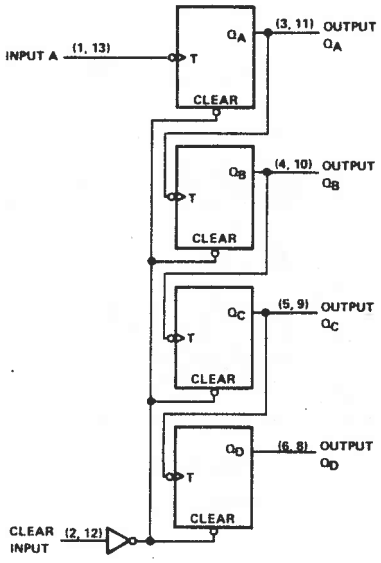
4.2.8 Dual Four-Bit Binary Counter (U10, U22, U34).

These devices contain eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package, each with a clear and clock input. Parallel outputs are available from each counter so that any submultiple of the input count frequency is available. See Figure 4-10 for logic diagram and truth table.

Connection Diagram



Logic Diagram



Truth Table

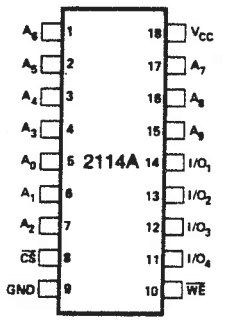
COUNT SEQUENCE (EACH COUNTER)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

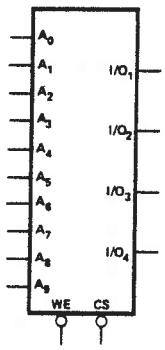
Figure 4-10. Four-Bit Binary counter Connections.

4.2.9 1024 X 4 Bit Static Random Access Memory (U17-U20, U29-U32). This device is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits and requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided and a separate chip select ($\overline{CS}$) lead allows easy selection of an individual package. For logic and connections, see Figure 4-11.

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
I/O_1–I/O_4	DATA INPUT/OUTPUT		

Logic Diagram

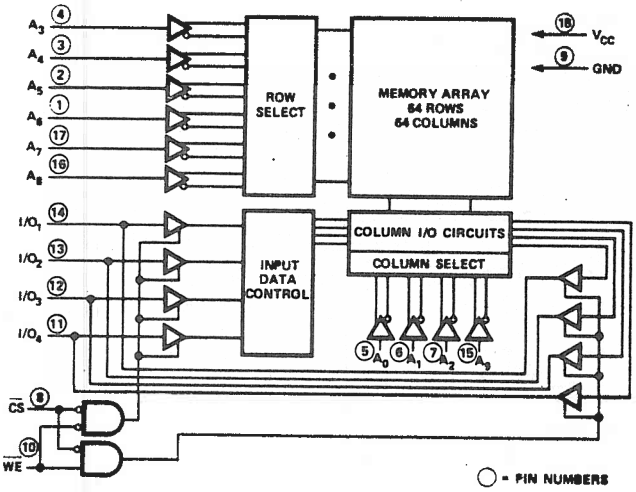
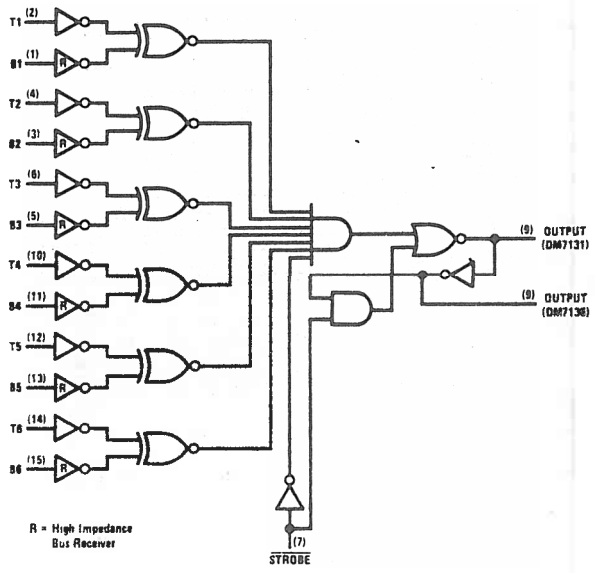


Figure 4-11. RAM Connections.

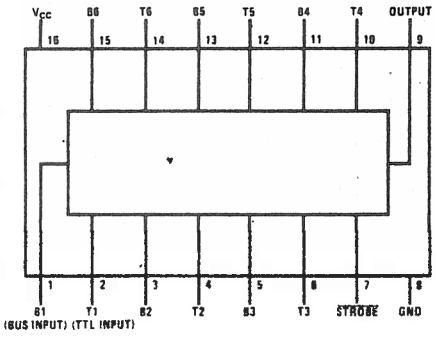
4.2.10 Bus Comparator (U37, U41, U42).

This device compares two binary words of two to six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are TTL inputs, whereas inputs of the second word are high impedance receivers driven by a terminated data bus. The output has a latch that is strobe controlled. The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logical 1 to a logical 0 state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logical 1 level, without affecting the state of the output. Logic and connections are shown in Figure 4-12.

Logic Diagram



Connection Diagram



Truth Table

CONDITION	$\overline{\text{STROBE}}$	OUTPUT	
		DM71/8131	DM71/8136
T = B, T ≠ B	H	Q_{N-1}*	Q_{N-1}*
T = B	L	L	H
T ≠ B	L	H	L

*Latched in previous state

Figure 4-12. Bus Comparator Connections.

SECTION V

MAINTENANCE AND TROUBLESHOOTING

5.0 INTRODUCTION.

The AM-320 circuit board performs to full capability with a minimum of maintenance. This section describes maintenance and troubleshooting procedures and procedures for handling warranty returns.

5.1 CIRCUIT BOARD CHECKOUT.

The AM-320 circuit board was fully tested before it left Alpha Microsystems and will operate satisfactorily in the system if the hardware and software requirements of Sections 2 and 3 of this manual are met. Should a problem arise, use the following procedures to identify and locate the fault.

1. Check all cables for proper seating of connectors.

2. Check each of the wires at the cable connectors to ensure that each wire is properly seated in its groove.

3. Check the circuit boards for proper seating in the slot.

4. Check all power connections for correct voltages.

5. Check jumper options to ensure correctness of application.

6. Verify that the fault is in the AM-320 and not either in the system or in the peripheral. This can best be accomplished with substitution of a known good circuit board.

7. Perform the diagnostic tests. Contact the Alpha Micro International Support/Services Group for details on diagnostic procedures and availability.

5.2 WARRANTY PROCEDURES.

This circuit board is covered by warranty issued by Alpha Microsystems Inc., Irvine, California. Complete details of the warranty are included with the circuit board. Should a problem arise with this circuit board, call your dealer or the Alpha Micro International Support/Services Group for information.

Table 6-1. AM-310 Cross Reference

REF. DESIG.	MFG. TYPE	PARA NO.	REF. DESIG.	MFG. TYPE	PARA. NO.
U1	8830	-	U26	74LS32	-
U2	7414	-	U27	74LS138	4.2.2
U3	8830	-	U28	74LS139	4.2.3
U4	8820	-	U29	2114	4.2.9
U5	8820	-	U30	2114	4.2.9
U6	74LS08	-	U31	2114	4.2.9
U7	74LS74	4.2.1	U32	2114	4.2.9
U8	74LS32	-	U33	74LS257	4.2.5
U9	74LS257	4.2.5	U34	74LS393	4.2.8
U10	74LS393	4.2.8	U35	74LS373	4.2.6
U11	8830	-	U36	NOT USED	-
U12	8830	-	U37	8131	4.2.10
U13	8830	-	U38	74LS374	4.2.7
U14	74LS32	-	U39	74LS244	4.2.4
U15	74LS74	4.2.1	U40	74LS244	4.2.4
U16	74LS74	4.2.1	U41	8131	4.2.10
U17	2114	4.2.9	U42	8131	4.2.10
U18	2114	4.2.9	U43	7805	-
U19	2114	4.2.9	U44	7805	-
U20	2114	4.2.9	U45	7805	-
U21	74LS257	4.2.5			
U22	74LS393	4.2.8			
U23	7437	-			
U24	2 MHz Osc.	-			
U25	74LS04	-			

REVISIONS				
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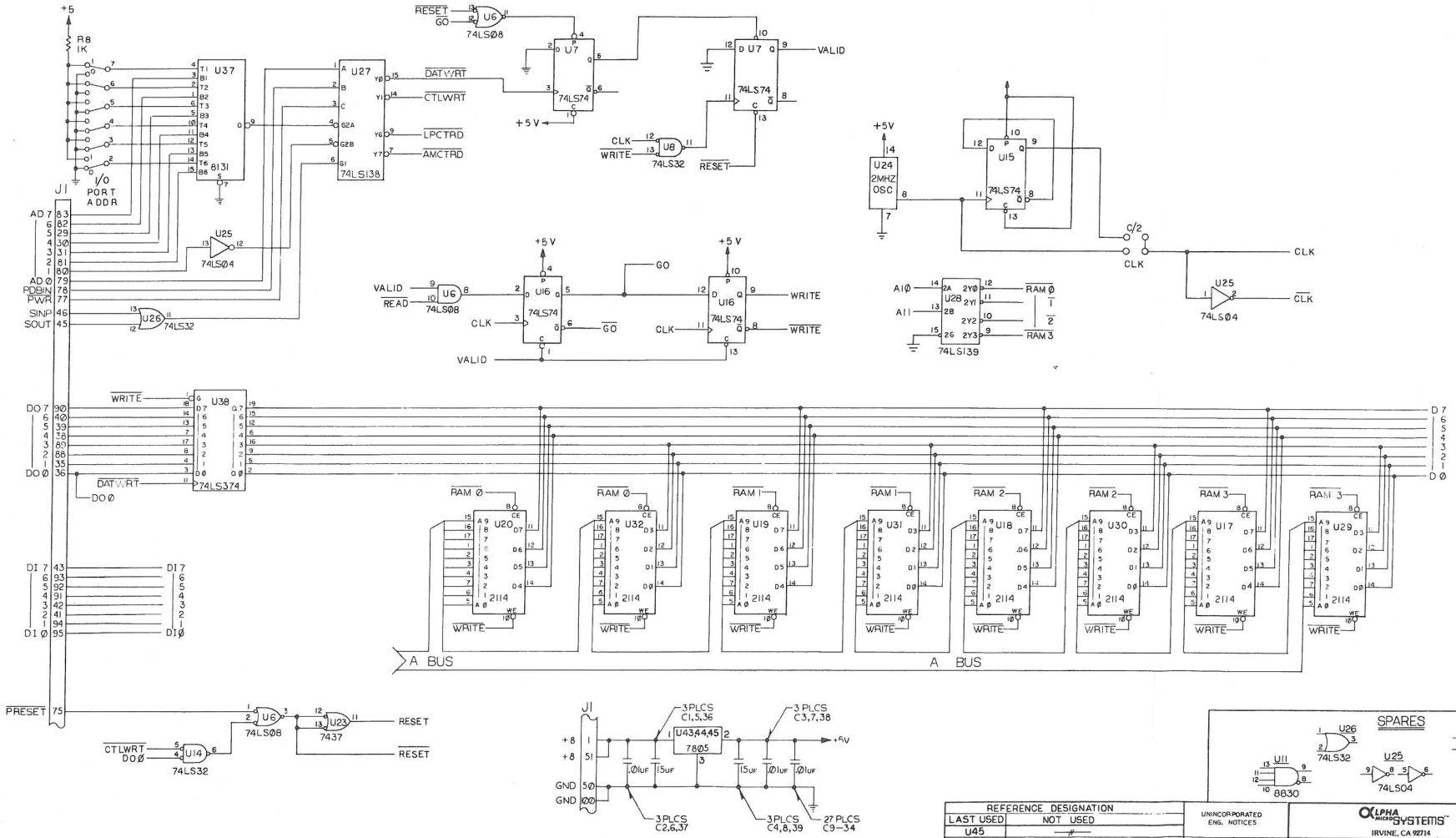
	B00	REL. PER EN00246	6/11/79	



SPARES

REFERENCE DESIGNATION	
LAST USED	NOT USED
U45	—
R8	—
C39	C35
J3	—

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1 OF 2

REVISIONS: P00

TITLE: AM 320 LINE PRINTER INTERFACE

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REVISIONS			
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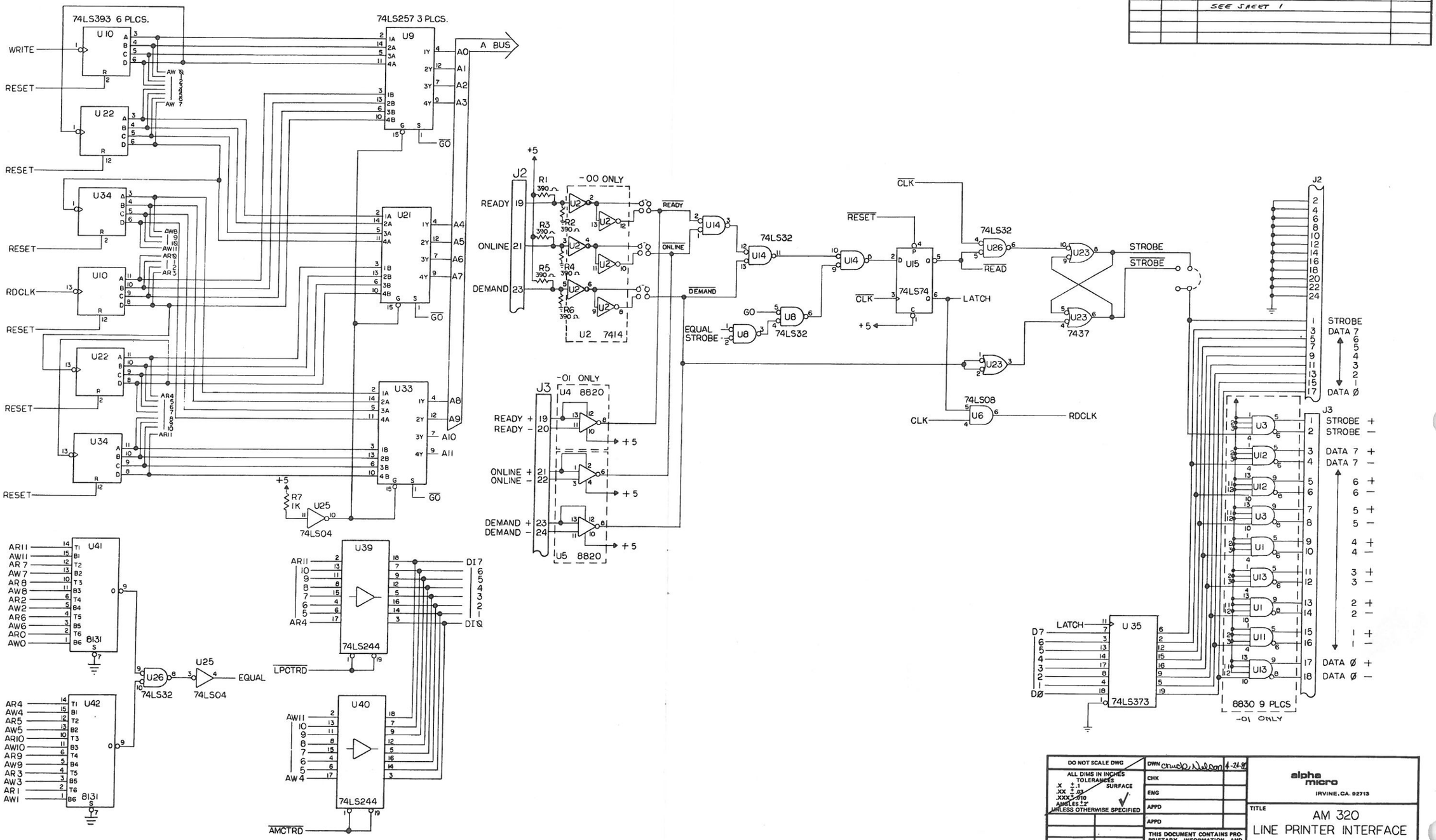
		SEE SHEET 1	



DO NOT SCALE DWG	DWN Orville Nelson 4-24-81	alpha micro	
ALL DIMS IN INCHES TOLERANCES X ±.1 XX ±.03 XXX ±.010 ANGLES ±2° UNLESS OTHERWISE SPECIFIED SURFACE ✓	CHK	IRVINE, CA. 92713	
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