DESIGN SPECIFICATION

AM-300

DWS-00300-00 REV. B00

alpha micro

REV. B00 | SH 1 | DWG. NO. DWS-00300-00

APPLICATION	
NEXT ASSY	USED ON

REVISIONS

REV.	DESCRIPTION	DATE	APPROVED
A00	RELEASED	10/18/78	
B00	REVISED PER EN 406	1-15-81	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.		alpha micro
MATERIAL	APPROVALS	DATE	AM-300 SIX PORT SERIAL INPUT/OUTPUT BOARD
	DRAWN J. GLADE	10/18/78	
FINISH	CHECKED		SIZE A · FSCM NO. · DWG. NO. DWS-00300-00 · REV. B00
	ISSUED		
DO NOT SCALE DRAWING			SCALE · SHEET 1 of 29

I. INTRODUCTION.

The Alpha Microsystem AM-300 Six Port Serial Input/Output Board has been designed to provide six programmable RS-232 I/O ports on a single printed circuit card.

The following is a summary of the AM-300 capability:

- S-100 bus compatible
- 6 fully programmable RS-232 I/O ports
- 16 selectable baud rates for each I/O port under software control (Max rate = 19,200 baud)
- Synchronous and asynchronous operating modes for each port utilizing versatile Western Digital Corporation Asynchronous Synchronous Receiver/Transmitter UC1671B)
- 5 CPU I/O ports utilized for data and control
- Multiple level interrupt compatibility

II. INSTALLATION INSTRUCTIONS.

A. AM-300 Board Options

1. I/O port address setting. Five CPU I/O ports are required by the AM-300. These I/O ports are defined in Tables I and II. The I/O port address is jumper settable in blocks of eight. Figure 1 illustrates the procedure for setting this address.

2. Vectored interrupt jumper setting. Each AM-300 board requires a separate vectored interrupt. Figure 2 illustrates the procedure for setting up the interrupt vector.

3. Clear to send (CTS) jumper option (Rev C or later boards only). Each RS-232 channel may be configured so that CTS is always asserted, or is controlled externally by the peripheral to which it is attached. Figure 3 illustrates these jumpers.

B. CPU Jumper Modifications

1. AM-100 CPU. If the system is an AM-100, vector interrupt jumpers for second and third AM-300 boards (VI6 and VI7) must be installed on CPU board No. 2. See Figure 4 for jumper placement. Note that no jumpers are required if only one AM-300 is installed in the system.

2. AM-100/T CPU. No modifications required.

C. AM-300 Board Installation

1. Install the AM-300 board into the closest available slot to the rear of the chassis.

2. Locate the three cables (DWB-10001-01) that accompanied the board and install the panel mount connectors into the CPU chassis rear panel using the hardware provided.

3. Install the edge connectors onto the AM-300 board edge fingers, keeping pin 1 on each connector toward the regulator end of the board. Note that the channel numbers on the AM-300 board will be as follows:

Edge Connector #1	RS-232 Conn #	Channel #
J2	1	1
	2	2
J3	1	3
	2	4
J4	1	5
	2	6

III. CPU I/O PORT DEFINITIONS.

Five CPU I/O ports are required by the AM-300. These are summarized in Tables I and II.

Note that the first four I/O addresses are contained in the Western Digital Corporation UC1671B ASTRO. See the data sheet on the chip for a detailed explanation of the register contents.

In addition to the registers contained in the UC1671B, there are three other functions that must be considered:

A. MUX Control Register

See Table II for description of control bits.

B. Baud Rate Programming

The baud rate for a given serial I/O channel can be programmed as follows:

1. Set up the MUX Control Register with bit 3 set to a "1" and bits 0-2 set to address the appropriate channel.

2. Write to port X0 with bits 0-3 used to select the appropriate baud rate. The Western Digital Dual Baud Rate Clock Generator (BR1941L) is utilized to provide the programmable baud rates. See the BR1941L spec sheet for detailed baud rate codes.

C. Interrupt Programming

Interrupts can be enabled by setting bit 4 of the MUX Control Register to a "1". Once set, any of the six channels can generate an interrupt to the CPU. A single line interrupt is used for *all* channels. To determine which channel has generated an interrupt, the following sequence must be programmed.

1. After receiving the interrupt, set up the MUX Control Register with bit 5 set on a "1" and bits 0-3 set to a "0".

2. Read port X0. The AM-300 will return the address of the channel that has generated the interrupt according to the following format:

Bit 7	MSB
Bit 6	
Bit 5	Interrupting
Bit 4	Channel Number
Bit 3	LSB
Bit 2	1 = Read Interrupt 0 = Write Interrupt

The channels have been prioritized such that I/O channel 1 has the highest priority and I/O channel 6 has the lowest.

IV. RS-232 INTERFACE.

Three edge connectors are provided at the top of the AM-300 to allow connection to RS-232 compatible peripherals. Each connector contains interface signals for two I/O channels. The following RS-232 signals are provided:

Inputs:

1. BB Received Data
2. CB Clear to Send
3. CC Data Set Ready
4. CF Carrier Detector

Outputs:

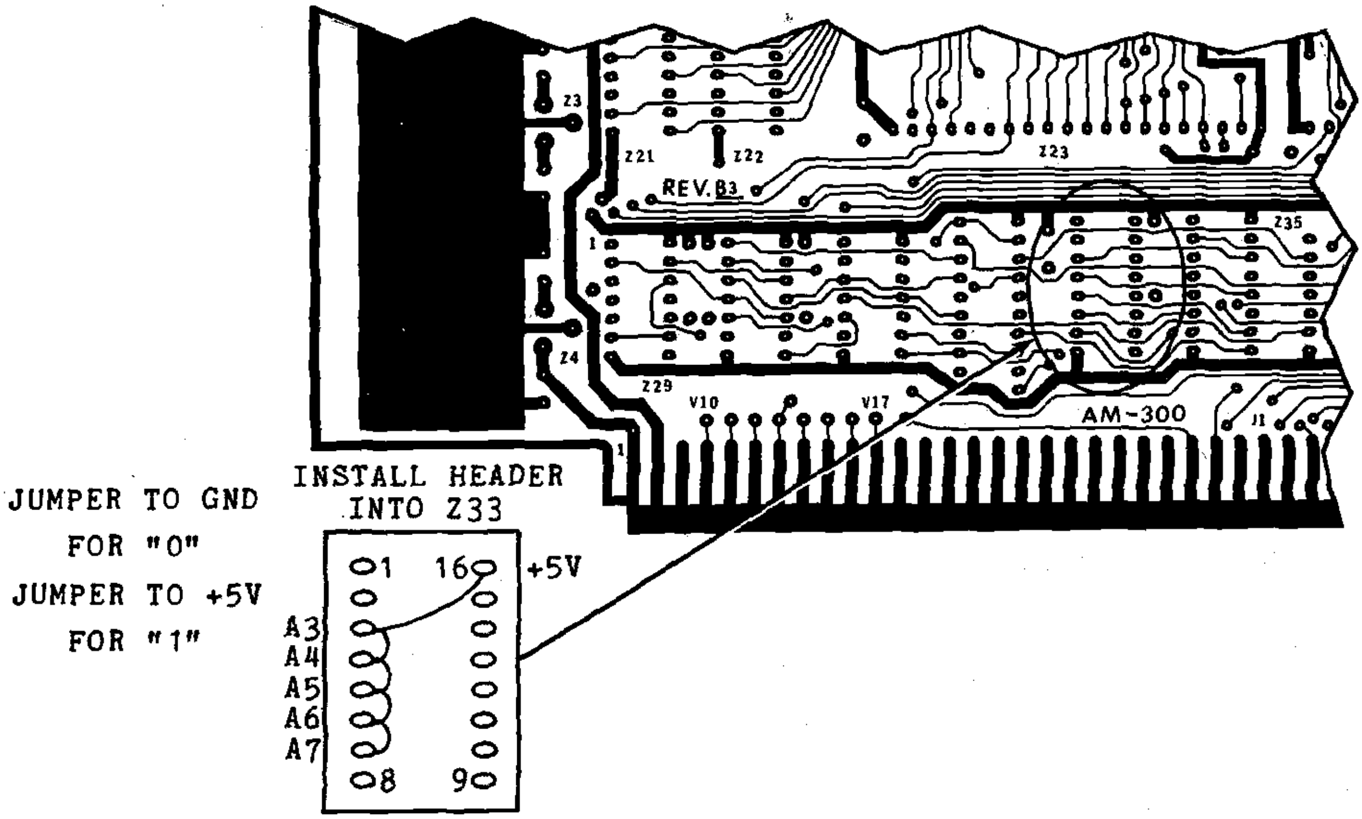
1. CD Data Terminal Ready
2. BA Transmitted Data
3. CA Request to Send
4. Misc Miscellaneous

Figure 5 illustrates the standard cable configuration.

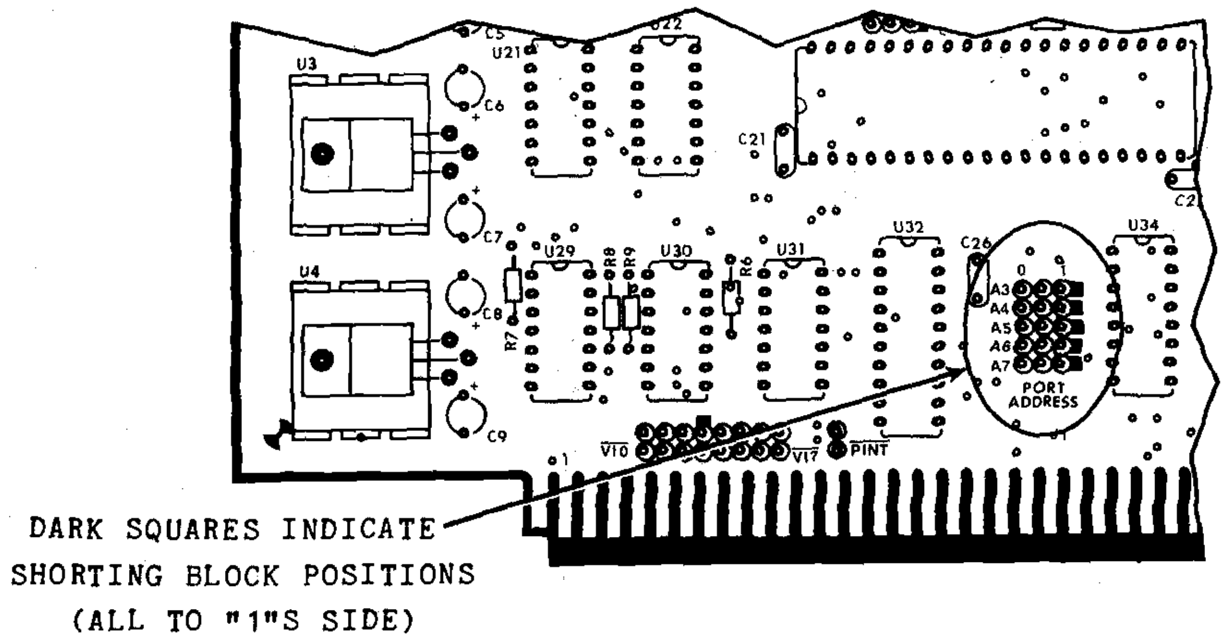
STANDARD I/O BASE ADDRESS IS :F8 (SHOWN)

2ND AM-300 I/O BASE ADDRESS IS :E8

3RD AM-300 I/O BASE ADDRESS IS :D8



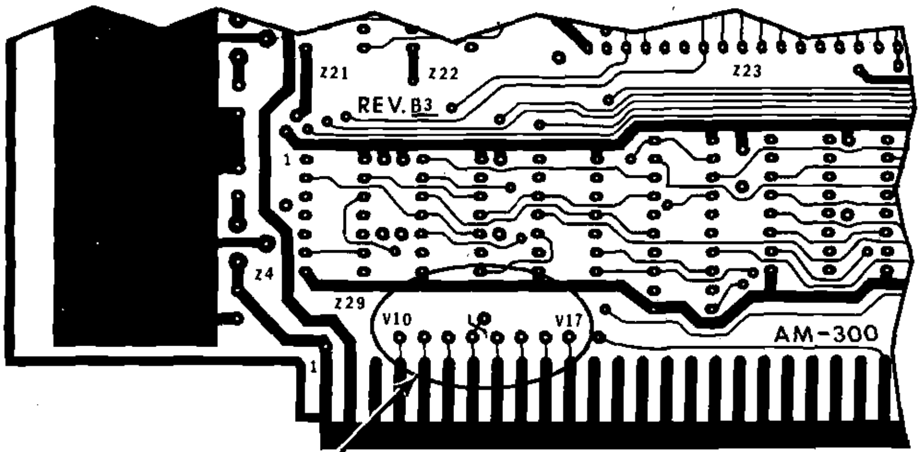
AM-300 I/O Port Address Jumper Setting (Board Rev A & B)



Board Rev C And Later

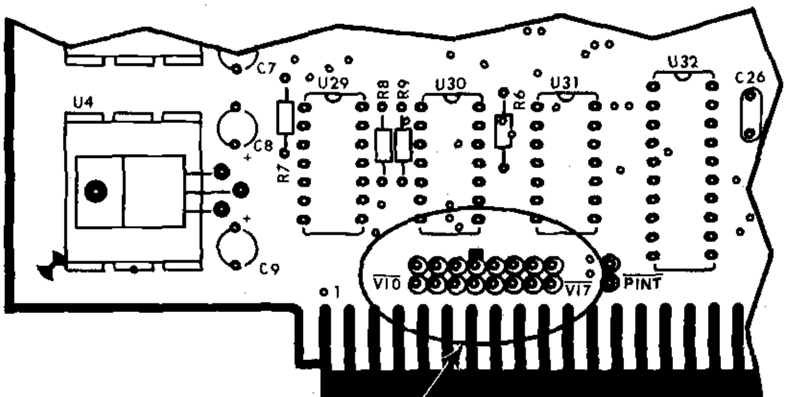
Figure 1

STANDARD VECTOR INTERRUPT IS LEVEL 3
2ND AM-300 VECTOR INTERRUPT IS LEVEL 6
3RD AM-300 VETOR INTERRUPT IS LEVEL 7



TO CHANGE FROM LEVEL 3
TO ANOTHER LEVEL, CUT ETCH ON COMPONENT
SIDE AS SHOWN AND JUMPER PAD TO DESIRED
VECTORED INTERRUPT LEVEL.

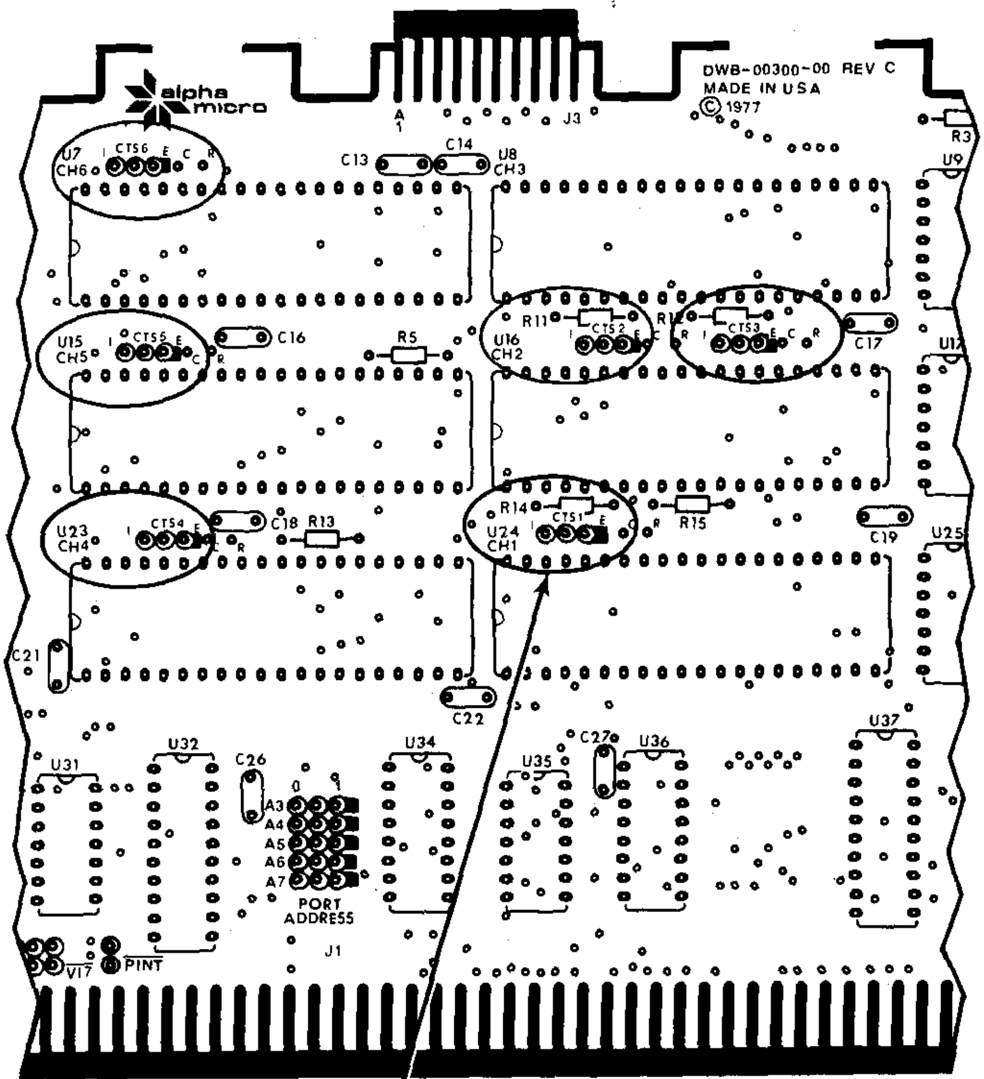
AM-300 Vector Interrupt Jumper Setting (Board Rev A & B)



DARK SQUARE INDICATES STANDARD
SHORTING BLOCK POSITION (LEVEL 3).
TO ALTER VECTOR INTERRUPT LEVEL, SIMPLY
REPOSITION SHORTING BLOCK TO DESIRED LEVEL.

Board Rev C And Later

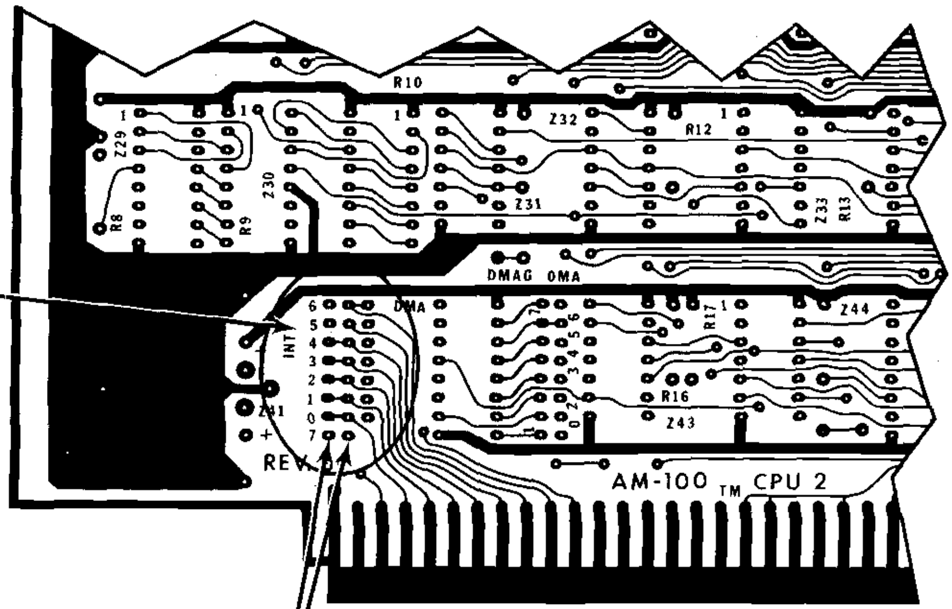
Figure 2



CTS JUMPERS, 6 PLACES
SHOWN BY DARK SQUARES IN THE
EXTERNAL POSITION (E).
INTERNAL POSITION (I) ALWAYS
ASSERTS CTS.

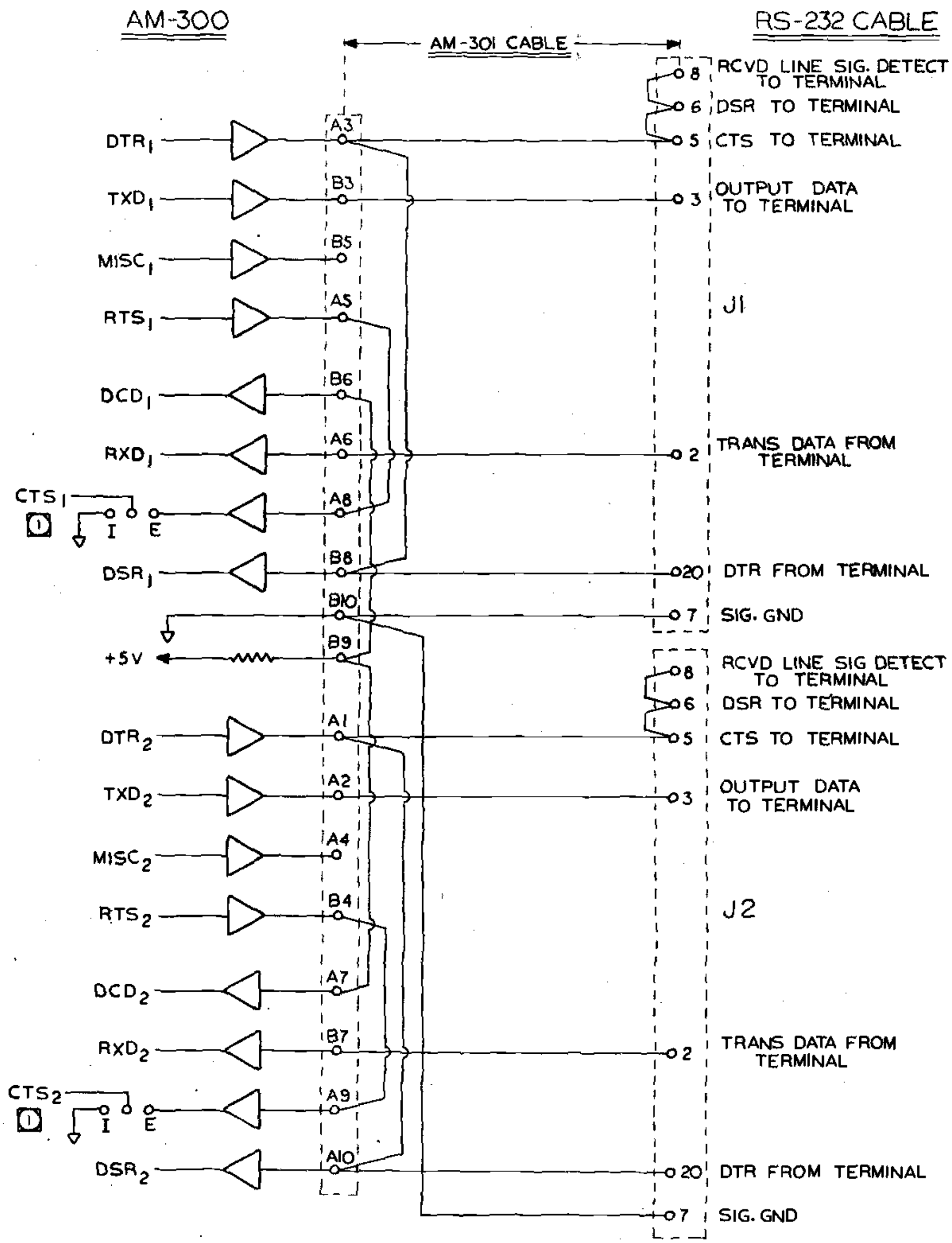
AM-300 CTS Jumper Options (Rev C And Later Boards Only)
Figure 3

INTERRUPT
LEVEL ID



INSTALL JUMPERS BETWEEN THESE COLUMNS OF PADS FOR THE APPROPRIATE INTERRUPT LEVELS BEING USED (0-7). NOTE THAT SOME JUMPERS ARE ALREADY ETCHED ONTO THE BOARD.

AM-100 Vector Interrupt Jumpers
Figure 4



1 JUMPER OPTION ON REV. C AND LATER BOARDS ONLY, REV. A AND B BOARDS ARE HARDWIRED TO "E" POSITION.

AM-300 Cabling Configuration
Figure 5

Table I. I/O Port Definitions

I/O Port Address ⚠1	Input	Output	Comments
X0	Control Register 1	Control Register 1	See UC1671B spec
X1	Control Register 2	Control Register 2	See UC1671B spec
X2	SYN and DLE Register	Status Register	See UC1671B spec
X3	Receiver Holding Register	Transmitter Holding Register	See UC1671B spec
X4	---------	MUX Control Register	See Table II

⚠1 the base I/O port address (shown as 0) is jumper selectable to any block of eight I/O addresses.

F8 = 248
E8 = 232
D8 = 216

Table II. MUX Control Register (X4)

	Bit	Function	Comments
1	0	Multiplex Control Bit 0	3 bit code addresse the appropriate RS-232 channel. Legal addresses are 1-6.
2	1	Multiplex Control Bit 1	
4	2	Multiplex Control Bit 2	
8	3	Program Baud Rate	Set to "1" to program addressed channel's baud rate. Set to "0" to program addressed channel's ASTRO.
16	4	Interrupt Enable	
32	5	Read Interrupt	Set to "1" to enable reading of interrupt vector.

WESTERN DIGITAL
C O R P O R A T I O N

BR1941 Dual Baud Rate Clock

AUGUST, 1980

FEATURES

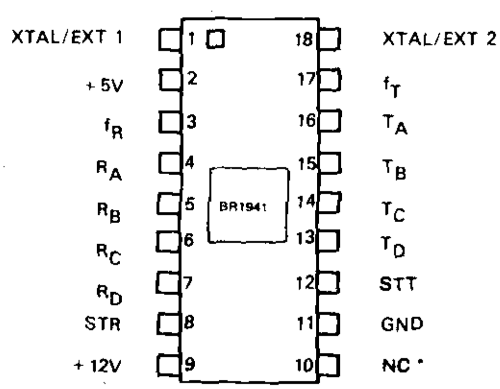
- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES
- DUAL SELECTABLE 16 X CLOCK OUTPUTS FOR FULL DUPLEX OPERATIONS
- OPERATES WITH CRYSTAL OSCILLATOR OR EXTERNALLY GENERATED FREQUENCY INPUT
- ROM MASKABLE FOR NON-STANDARD FREQUENCY SELECTIONS
- DIRECT UART/USRT AND TTL COMPATIBILITY
- OUTPUTS A 50% DUTY CYCLE CLOCK WITH 0.01% ACCURACY
- 18 PIN CERAMIC DIP PACKAGE
- 3 DIFFERENT FREQUENCY/DIVISOR PAIRS AVAILABLE

GENERAL DESCRIPTION

The BR1941 is a combination Baud Rate Clock Generator and Programmable Divider. It is manufactured in N-channel MOS using silicon gate technology. This device is capable of generating 16 externally selected clock rates whose frequency is determined by either a single crystal or an externally generated input clock. The BR1941 is a programmable counter capable of generating a division from 2 to $(2^{15}-1)$.

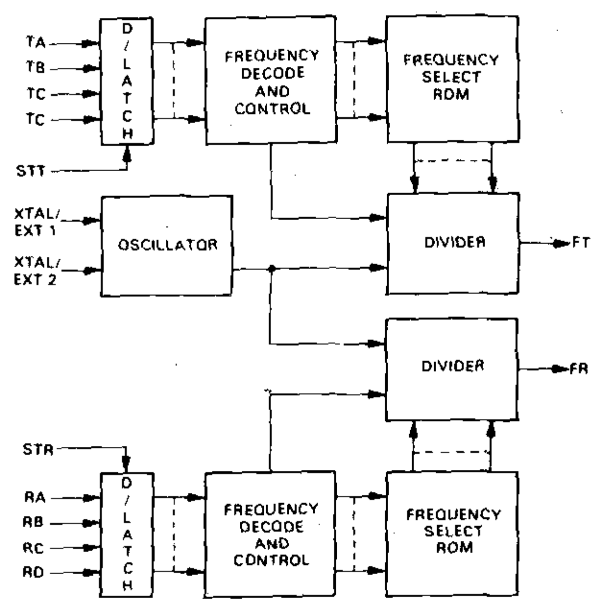
The BR1941 is available programmed with the most used frequencies in data communication. Each frequency is selectable by strobing or hard wiring each of the two sets of four Rate Select inputs. Other frequencies/division rates can be generated by reprogramming *the internal ROM coding through a MOS mask change.* Additionally, further clock division may be accomplished through cascading of devices. The frequency output is fed into the XTAL/EXT input on a subsequent device.

The BR1941 can be driven by an external crystal or by TTL logic. All pins are TTL compatible.



*INTERNALLY BONDED. DO NOT CONNECT ANYTHING TO THIS PIN.

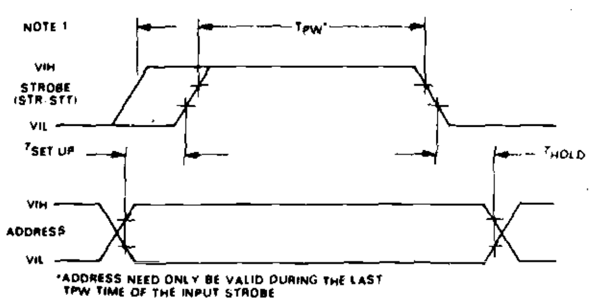
PIN CONNECTIONS



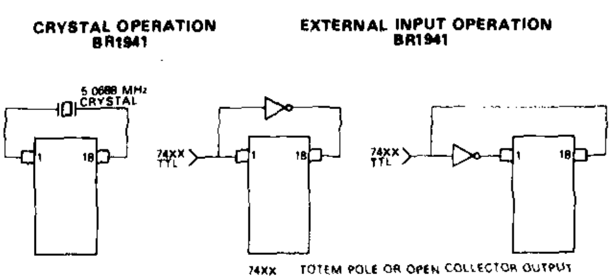
BR1941 BLOCK DIAGRAM

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	XTAL/EXT 1	Crystal or External Input 1	This input receives one pin of the crystal package or or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt Supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver Address inputs.
4-7	R_A, R_B, R_C, R_D	Receiver Address	The logic level on these inputs as shown in Table 1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_A, R_B, R_C, R_D) into the receiver address register This input may be strobed or hard wired to +5V.
9	V_{DD}	Power Supply	+12 volt Supply
10	NC	No Connection	Internally bonded.Do not connect anything to this pin.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T_A, T_B, T_C, T_D) into the transmitter address register. This input may be strobed or hard wired to +5V.
13-16	T_D, T_C, T_B, T_A	Transmitter Address	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter Address inputs.
18	XTAL/EXT 2	Crystal or External Input 2	This input receives the other pin of the crystal package or the other polarity of the external input.



CONTROL TIMING



CRYSTAL/CLOCK OPTIONS

MAXIMUM RATINGS

Operating Temperature Range	0°C to +70°C
Positive Voltage on any Pin, with respect to ground	+20.0V
Negative Voltage on any Pin, with respect to ground	-0.3V
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+325°C

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and Functional Operation of the device at these or at any other condition above those indicated in the operational sections of this specification are not implied.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ± 5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding XTAL inputs
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 3.2 mA
High-level, V_{OH}	V_{CC}-1.5	4.0		V	I_{OH} = 100 μA
INPUT CURRENT					
Low-level, I_{IL}			0.3	mA	V_{IN} = GND, excluding XTAL inputs
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = GND, excluding XTAL inputs
EXT INPUT LOAD		*4*			
POWER SUPPLY CURRENT					
I_{CC}		20			
I_{DD}		20			
AC CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY		5.0688		MHz	XTAL, EXT
PULSE WIDTH (T_{PW})					
Clock					50% Duty Cycle ± 10%
Receiver strobe	150		DC	ns	See Note 1
Transmitter strobe	150		DC	ns	See Note 1
INPUT SET-UP TIME (T_{SET-UP}) Address	50			ns	See Note 1
OUTPUT HOLD TIME(T_{HOLD}) Address	50			ns	

NOTE 1: Input set-up time can be decreased to >0 ns by increasing the minimum strobe width by 50 ns to a total of 200 ns.
All inputs except XTAL/EXT have internal pull-up resistors.

OPERATION

Standard Frequencies

Choose a Transmitter and receiver frequency from the table below. Program the corresponding address into TA-TD and RA-RD respectively using 200 nsec minimum strobe pulses or by hard wiring the strobe and address inputs.

Non-Standard Frequencies

To accomplish non-standard frequencies do one of the following:

1. Choose a crystal that when divided by the BR1941 generates the desired frequency.
2. Cascade devices by using the frequency outputs as an input to the XTAL/EXT inputs of the subsequent BR1941.
3. Consult the factory for possible changes via ROM mask reprogamming.

TABLE 4. CRYSTAL FREQUENCY = 4.2130 MHZ

Transmit/Receive Address				Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
1	0	0	0	50	0.8	0.80004	.005	50/50	5266
0	0	0	1	75	1.2	1.19995	.004	50/50	3511
0	0	1	0	110	1.76	1.759828	.0097	50/50	2394
0	0	1	1	134.5	2.152	2.1517	.014	50/50	1958
0	1	0	0	150	2.4	2.40059	.025	50/50	1755
0	1	0	1	200	3.2	3.19896	.003	50/50	1317
0	1	1	0	300	4.8	4.79844	.033	50/50	878
1	1	1	1	600	9.6	9.59688	.033	49.9/50.1	439
1	0	0	0	1050	16.8	16.7849	0.95	49.8/50.2	251
1	0	0	1	1200	19.2	19.2376	.196	49.8/50.2	219
1	0	1	0	1800	28.3	28.8564	.194	50/50	146
1	0	1	1	2000	32.0	31.9169	.26	50/50	132
1	1	0	0	2400	38.4	38.3003	.26	50/50	110
1	1	0	1	4800	76.8	76.6	.2	49/51	55
1	1	1	0	9600	153.6	156.04	1.56	48/52	27
1	1	1	1	19200	307.2	300.93	2.04	50/50	14

*When the duty cycle is not exactly 50% it is 50% ± 10%

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TABLE 1. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16× Clock	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.83	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

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TABLE 3. CRYSTAL FREQUENCY = 4.9152 MHZ

Transmit/Receive Address				Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7598	-0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	-0.19	*	171
1	0	0	1	2000	32.0	31.9168	-0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	-0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

*When the duty cycle is not exactly 50% it is 50% ± 10%

BR1941-07

TABLE 2. CRYSTAL FREQUENCY 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical Frequency 32X Clock	Actual Frequency 32X Clock	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	1.6 KHz	1.6 KHz	—	50/50	3168
0	0	0	1	75	2.4	2.4	—	50/50	2112
0	0	1	0	110	3.52	3.52	—	50/50	1440
0	0	1	1	134.5	4.304	4.303	.026	50/50	1178
0	1	0	0	150	4.8	4.8	—	50/50	1056
0	1	0	1	200	6.4	6.4	—	50/50	792
0	1	1	0	300	9.6	9.6	—	50/50	528
0	1	1	1	600	19.2	19.2	—	50/50	264
1	0	0	0	1200	38.4	38.4	—	50/50	132
1	0	0	1	1800	57.6	57.6	—	50/50	88
1	0	1	0	2400	76.8	76.8	—	50/50	66
1	0	1	1	3600	115.2	115.2	—	50/50	44
1	1	0	0	4800	153.6	153.6	—	*	33
1	1	0	1	7200	230.4	230.4	—	50/50	22
1	1	1	0	9600	307.2	298.16	2.941	*	17
1	1	1	1	19,200	614.4	633.6	3.125	50/50	8

*When the duty cycle is not exactly 50% it is 50% ± 10%

BR1941-06

TABLE 5. CRYSTAL FREQUENCY = 4.9152 MHZ

Transmit/Receive Address				Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Divisor
A	B	C	D					
0	0	0	0	50	0.8 KHz	0.8 KHz	—	6336
0	0	0	1	75	1.2	1.2	—	4224
0	0	1	0	110	1.76	1.76	—	2880
0	0	1	1	150	2.4	2.4	—	2112
0	1	0	0	200	3.2	3.2	—	1584
0	1	0	1	300	4.8	4.8	—	1056
0	1	1	0	600	9.6	9.6	—	528
0	1	1	1	1050	16.8	16.784	0.095	302
1	0	0	0	1200	19.2	19.2	—	264
1	0	0	1	1800	28.8	28.8	—	176
1	0	1	0	2000	32.0	32.081	0.253	158
1	0	1	1	2400	38.4	38.4	—	132
1	1	0	0	4800	76.8	76.8	—	66
1	1	0	1	7200	115.2	115.2	—	44
1	1	1	0	9600	153.6	153.6	—	33
1	1	1	1	19,200	307.2	316.8	3.125	16

*When the duty cycle is not exactly 50% it is 50% ± 10%

BR1941-11

WESTERN DIGITAL
C O R P O R A T I O N

UC1671 Asynchronous/Synchronous Receiver/Transmitter

JUNE, 1980

FEATURES

SYNCHRONOUS AND ASYNCHRONOUS
- Full Duplex Operations

SYNCHRONOUS MODE
- Selectable 5-8 Bit Characters
- Two Successive SYN Characters Sets Synchronization
- Programmable SYN and DLE Character Stripping
- Programmable SYN and DLE-SYN Fill

ASYNCHRONOUS MODE
- Selectable 5-8 Bit Characters
- Line Break Detection and Generation
- 1-, 1½-, or 2-Stop Bit Selection
- False Start Bit Detection
  Automatic Serial Echo Mode

SYSTEM COMPATIBILITY
- Double Buffering of Data
- 8-Bit Bi-Directional Bus For Data, Status, and Control Words
- All Inputs and Outputs TTL Compatible
- Up to 32 ASTROS Can Be Addressed On Bus
- On-Line Diagnostic Capability

TRANSMISSION ERROR DETECTION-PARITY
Overrun and Framing

BAUD RATE — DC TO 1M BAUD/SEC

8 SELECTABLE CLOCK RATES
- Accepts 1X Clock and Up to 4 Different 32X Baud Rate Clock Inputs
- Up to 47% Distortion Allowance with 32X Clock

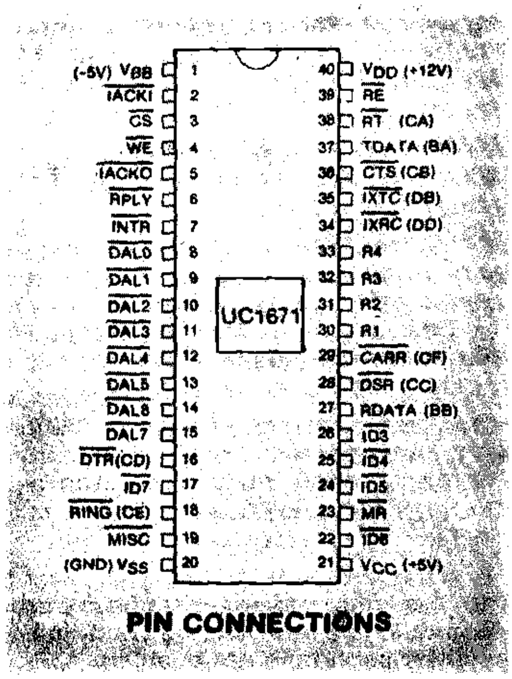
APPLICATIONS

SYNCHRONOUS COMMUNICATIONS
ASYNCHRONOUS COMMUNICATIONS
SERIAL/PARALLEL COMMUNICATIONS

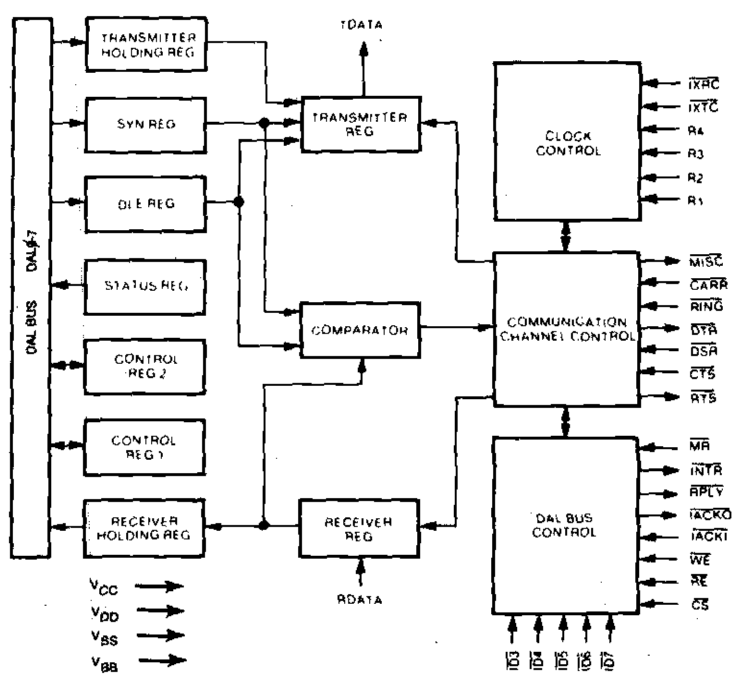
GENERAL DESCRIPTION

The UC1671B (ASTRO) is a MOS/LSI device which performs the functions of interfacing a serial data communication channel to a parallel digital system. The device is capable of full duplex communications (receiving and transmitting) with synchronous or asynchronous systems. The ASTRO is designed to operate on a multiplexed bus with other bus-oriented devices. Its operation is programmed by a processor or controller via the bus and all parallel data transfers with these machines are accomplished over the bus lines.

The ASTRO is fabricated in n-channel silicon gate MOS technology and is TTL compatible on all inputs and outputs.



PIN CONNECTIONS



UC1671 BLOCK DIAGRAM

PIN OUTS

The device is packaged in a 40-pin plastic or ceramic cavity package. The interface signals are defined below with all input/output signals complemented to facilitate bussing and interfacing with TTL. The Data Set controls and Status signals are also complemented to allow for an inversion when converting to EIA RS232C levels. The names and symbols assigned to the Data Set interface signals follows EIA standard nomenclature.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	POWER SUPPLIES	V_{BB}	−5V
21		V_{CC}	+5V
40		V_{DD}	+12V
20		V_{SS}	Ground
23	MASTER RESET	$\overline{MR}$	The Control and Status Registers and other controls are cleared when this input is low.
8-15	DATA ACCESS LINES	$\overline{DAL0\text{-}DAL7}$	Eight-bit bi-directional bus used for transfer of data, control, status, and address information.
17,22,24, 25,26	SELECT CODE	$\overline{ID7\text{-}ID3}$	Five input pins which when hard-wired assign the device a unique identification code used to select the device when addressing and used as an identification when responding to interrupts.
3	CHIP SELECT	$\overline{CS}$	The low logic transition of CS identifies a valid address on the DAL bus during Read and Write operations.
39	READ ENABLE	$\overline{RE}$	This signal, when low, gates the contents of an addressed register from a selected ASTRO onto the DAL.
4	WRITE ENABLE	$\overline{WE}$	This signal, when low, gates the contents of the DAL bus into the addressed register of a selected ASTRO.
7	INTERRUPT	$\overline{INTR}$	This open drain output is made low when one of the communication interrupt conditions occur.
2	INTERRUPT ACKNOWLEDGE IN	$\overline{IACKI}$	This input becomes low when polling takes place on the bus by the Controller to determine the interrupting source. When this signal is received, the ASTRO places its ID code on the DAL if it is requesting interrupt, otherwise it makes IACKO a low.
5	INTERRUPT ACKNOWLEDGE OUT	$\overline{IACKO}$	This output is made a logic low in response to a low IACKI if the ASTRO receiving an IACKI input is not the interrupting device.
6	REPLY	$\overline{RPLY}$	This open drain output is made low when the ASTRO is responding to being selected by an address on the DAL during read or write operations or in affirming that it is the interrupting source during interrupt polling.
30-33	CLOCK RATES	R1-R4	These four inputs accept four different local 32X data rate Transmit and Receive clocks. The input on R4 may be divided down into a 32X clock from a 32X, 64X, 128X, or 256X clock input. The clock used in the ASTRO is selected by the Control Register.
37	TRANSMITTED DATA	TDATA (BA)	This output is the transmitted serial data from the ASTRO. This output is held in a Marking condition when the transmitter section is not enabled.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
27	RECEIVED DATA	RDATA (BB)	This input receives serial data into the ASTRO.
38	REQUEST TO SEND	$\overline{\text{RTS}}$ (CA)	This output is enabled by the Control Register and remains in a low state during transmitted data from the ASTRO.
36	CLEAR TO SEND	$\overline{\text{CTS}}$ (CB)	This input, when low, enables the transmitter section of the ASTRO.
28	DATA SET READY	$\overline{\text{DSR}}$ (CC)	This input generates an interrupt when going On or Off while the Data Terminal Ready signal is On. It appears as a bit in the Status Register.
16	DATA TERMINAL READY	$\overline{\text{DTR}}$ (CD)	This output is generated by a bit in the Control Register and indicates Controller readiness.
18	RING INDICATOR	$\overline{\text{RING}}$ (CE)	This input from the Data Set generates an interrupt when made low with Data Terminal Ready in the "Off" condition.
29	CARRIER DETECTOR	$\overline{\text{CARR}}$ (CF)	This input from the Data Set generates an interrupt when going On or Off if Data Terminal Ready is On. It appears as a bit in the Status Register.
35	TRANSMITTER TIMING	$\overline{\text{IXTC}}$ (DB)	This input is the Transmitter 1X Data Rate Clock. Its use is selected by the Control Register. The transmitted data changes on the negative transition of this signal.
34	RECEIVER TIMING	$\overline{\text{IXRC}}$ (DD)	This input is the Receiver 1X Data Rate Clock. Its use is selected by the Control Register. The Received Data is sampled by the ASTRO on the positive transition of this signal.
19	MISCELLANEOUS	$\overline{\text{MISC}}$	This output is controlled by a bit in the Control Register and is used as an extra programmable signal.

RECEIVER REGISTER — This 8-bit shift register inputs the received data at a clock rate determined by the Control Register. The incoming data is assembled to the selected character length and then transferred to the Receiver Holding Register with logic zeroes filling out any unused high-order bit positions.

RECEIVER HOLDING REGISTER — This 8-bit parallel buffer register presents assembled receiver characters to the DAL bus lines when requested through a Read operation.

COMPARATOR — The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register and the SYN register or DLE register. A match between the registers sets up stripping of the received character, when programmed, by preventing the data from being loaded into the Receiver Holding Register. A bit in the Status Register is set when stripping is performed. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

SYN REGISTER — This 8-bit register is loaded from the DAL lines by a Write operation and holds the synchronization code used to establish receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Holding Register during transmission. This register cannot be read onto the DAL lines. It must be loaded with logic zeroes in all unused high-order bits.

DLE REGISTER — This 8-bit register is loaded from the DAL lines by a Write operation and holds the "DLE" character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the ASTRO may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode.

TRANSMITTER HOLDING REGISTER — This 8-bit parallel buffer register holds parallel transmitted data transferred from the DAL lines by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is ready to send new data.

TRANSMITTER REGISTER — This 8-bit shift register is loaded from the Transmitter Holding Register, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the transmitted Data output.

CONTROL REGISTERS — There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the DAL lines by a Write operation or read onto the DAL lines by a Read operation. The registers are cleared by a Master Reset.

STATUS REGISTER — This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the DAL lines by a Read operation.

DATA ACCESS LINES — The DAL is an 8-bit bidirectional bus port over which all address, data, control, and status transfers occur. In addition to transferring data and control words the DAL lines also transfer information related to addressing of the device, reading and writing requests, and interrupting information.

ASTRO OPERATION

ASYNCHRONOUS MODE

Framing of asynchronous characters is provided by a Start bit (logic low) at the beginning of a character and a Stop bit (logic high) at the end of a character. Reception of a character is initiated on recognition of the first Start bit by a positive transition of the receiver clock, after a preceding Stop bit. The Start and Stop bits are stripped off while assembling the serial input into a parallel character.

The character assembly is completed by the reception of the Stop bit after reception of the last character bit. If this bit is a logic high, the character is determined to have correct framing and the ASTRO is prepared to receive the next character. If the Stop bit is a logic low the Framing Error Status flag is set and the Receiver assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still a logic low when sampled at the theoretical center of the assumed Start bit. As long as the Receive input is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeroes is assembled along with a zero in the Stop bit location, the first received logic high is determined as a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Holding Register is transferred to the Transmitter Register. Transmission is initiated by the insertion of a Start bit, followed by the serial output of the character least significant bit first with parity, if enabled, following the most significant bit; then the insertion of a 1-, 1.5-, or 2-bit length Stop condition. If the Transmitter Holding Register is full, the next character transmission starts after the transmission of the Stop bit of the present character in the Transmitter Register. Otherwise, the Mark (logic high) condition is continually transmitted until the Transmitter Holding Register is loaded.

In order to allow re-transmission of data received at a slightly faster character rate, means are provided for shortening the Stop bit length to allow transmission of characters to occur at the same rate as the reception of characters. The Stop bit is shortened by 1/16 of a bit period for 1-Stop bit selection and 3/16 of a bit period for 1.5-, or 2-Stop bit selection, if the next character is ready in the Transmitter Holding Register.

SYNCHRONOUS MODE

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two continuous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Holding Register, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by contents of the Control Register. If, after the first SYN character detection, a second SYN character is present, the Receiver enters the Synchronization mode until the Receiver Enable Bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters are transmitted once the Transmitter is enabled. If the Transmitter Holding Register is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Non-transparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transparent mode of operation.

DETAILED OPERATION

Receiver — The Receiver Data input is clocked into the Receiver Register by a 1X Receiver Clock from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs. When using the 1X clock, the *Receiver* Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receive Sampling Clock is phased to the Mark-To-Space transition of the Received Data Start bit and defines, through clock counts, the center of each received Data bit within +0%, −3% at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all Mark-To-Space transitions of the Received Data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the Sampling Clock by 1/32nd of a bit period. The Sampling Clock can be immediately phased to every Mark-To-Space Data transition by setting Bit 4 of Control Register 1 to a logic high, while the Receiver is disabled.

When the complete character has been shifted into the Receiver Register it is then transferred to the Receiver Holding Register; the unused, higher number bits are filled with zeroes. At this time the Receiver Status bits (Framing Error/Sync Detect, *Parity Error/DLE Detect, Overrun Error,* and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered while the Receiver parity check is enabled in the Control Register. Overrun Error is set if the Data Received status bit is not cleared through a Read operation by an external device when a new character is ready to be transferred to the Receiver Holding Register. This error flag indicates that a character has been lost, as new data is lost and the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the contents of the SYN or DLE register are not loaded into the Receiver Holding Register, and the DR interrupt is not generated, if Bit 3 of Control Register 2 (CR23 = SYN Strip) or Bit 4 of Control Register 1 (CR14 = DLE Strip) are set respectively, the SYN-DET and DLE-DET status bits are set with the next non SYN or DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received only the first DLE character is stripped. No parity check is made while in this mode.

Transmitter — Information is transferred to the Transmitter Holding Register by a Write operation. Information can be loaded into this register at any time, even when the Transmitter is not enabled. Transmission of data is initiated only when the Request To Send bit is set to a logic one in the Control Register and the $\overline{\text{Clear To Send}}$ input is a logic low. Information is normally transferred from the Transmitter Holding Register to the Transmitter Register when the latter has completed transmission of a character. However, information in the *DLE register may be transferred* prior to the information contained in the Transmitter Holding Register if the Force DLE signal condition is enabled (Bits 5 = Force DLE and 6 = TX Transparent of Control Register 1 set to a logic one). The control bit CR15 must be set prior to loading of a new character in the transmitter holding register to insure forcing the DLE character *prior to transmission* of the *data* character. The Transmitter Register output passes through a flip-flop which delays the output by one clock period. When using the 1X clock generated by the Modem Data Set, the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock the transmitter section selects one of the four selected *rate inputs* and *divides the clock down to the baud* rate. This clock is phased to the Transmitter Holding Register empty flag such that transmission of characters occurs within two clock times of the loading of the Transmitter Holding Register when the Transmitter Register is empty.

When the Transmitter is enabled, a Transmitter interrupt is generated each time the Transmitter Holding Register is empty. If the Transmitter Holding Register is empty when the Transmitter Register is ready for a new character the Transmitter enters an idle state. During this idle time a logic high will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN register will be presented in the Synchronous Non-transparent mode (CR16 = 0). In the Synchronous Transmit Transparent mode (enabled by Bit 6 of Control Register 1 = Logic 1), the idle state will be filled by a DLE-SYN character transmission in that order. When entering the Transparent mode the DLE-SYN fill will not occur until the first forced DLE.

If the Transmitter section is disabled by a reset of the Request to Send, any partially transmitted character is completed before the transmitter section of the ASTRO is disabled. As soon as the CTS goes high the transmitted data output will go high.

When the Transmit parity is enabled, the selected Odd or Even parity bit is inserted into the last bit of the character in place of the last bit of the Trans*mitted Register.* This *limits transfer of character* information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transparency mode.

DEVICE PROGRAMMING

The two 8-bit Control Registers *of the* ASTRO determine the operative conditions of the ASTRO chip. Control Register 1 is shown in the following table.

128	64	32	16	8	4	2	1
BIT 7 7	6	5	4	3	2	1	0
SYNC/ASYNC 0—LOOP MODE 1—NORMAL MODE	ASYNC 0—NON BREAK MODE 1—BREAK MODE SYNC 0—NON TRANSMITTER TRANSPARENT MODE 1—TRANSMIT TRANSPARENT MODE	ASYNC (TRANS. ENABLED) 0—1 1/2 or 2 STOP BIT SELECTION 1—SINGLE STOP BIT ASYNC (TRANS. DISABLED) 0—$\overline{\text{MISC}}$ OUT = 1 1—$\overline{\text{MISC}}$ OUT = 0 SYNC (CR16 = 0) 0—NO PARITY GENERATED 1—TRANSMIT PARITY ENABLED SYNC (CR16 = 1) 0—NO FORCE DLE 1—FORCE DLE	ASYNC 0—NON ECHO MODE 1—AUTO ECHO MODE SYNC (CR12 = 1) 0—DLE STRIPPING NOT ENABLED 1—DLE STRIPPING ENABLED SYNC (CR12 = 0) 0—$\overline{\text{MISC}}$ OUT = 1 1—$\overline{\text{MISC}}$ OUT = 0	ASYNC 0—NO PARITY ENABLED 1—PARITY CHECK ENABLED ON RECEIVER PARITY GENERATION ENABLED ON TRANSMITTER SYNC 0—RECEIVER PARITY CHECK IS DISABLED 1—RECEIVER PARITY CHECK IS ENABLED	SYNC/ASYNC 0—RECEIVER DISABLED 1—RECEIVER ENABLED	SYNC/ASYNC 0—SETS $\overline{\text{RTS}}$ OUT = 1 1—SET $\overline{\text{RTS}}$ OUT = 0	SYNC/ASYNC 0—SET $\overline{\text{DTR}}$ ~~OUT = 1~~ 1—SETS $\overline{\text{DTR}}$ OUT = 0

CONTROL REGISTER 1

Control Register 1

Bit 7 — A logic 0 configures the ASTRO into an Internal Data and Control Loop mode and disables the Ring interrupt. In this diagnostic mode the following loops are connected internally:

a. The Transmit Data is connected to the Receive Data with the TD pin held in a Mark condition and the input to the RD pin disregarded.

b. With a 1X clock selected, the Transmitter Clock also becomes the Receive Clock.

c. The Data Terminal Ready (DTR) Control bit is connected to the Data Set Ready (DSR) input, with the $\overline{\text{DTR}}$ output in held in an Off condition (logic high), and the $\overline{\text{DSR}}$ input pin is disregarded.

d. The Request to Send Control bit is connected to the Clear To Send ($\overline{\text{CTS}}$) and Carrier Detector inputs, with the $\overline{\text{RTS}}$ output pin held in an Off condition (logic high), and the $\overline{\text{CTS}}$ and Carrier Detector input pins are disregarded.

e. The Miscellaneous pin is held in an Off (logic high) condition.

A logic 1 on Bit 7 enables the Ring interrupt and returns the ASTRO to the normal full duplex configuration.

Bit 6 — In the *Asychronous* mode a logic 1 holds the Transmitted Data output in a Spacing (Logic 0) condition, starting at the end of any current transmitted character, when the Transmitter is enabled. Normal Transmitter timing continues so that this Break condition can be timed out after the loading of new characters into the Transmitter Holding Register.

In the *Synchronous* mode a logic 1 sets the Transmitter in a transparent transmission which implies that idle transmitter time will be filled by DLE-SYN character transmission and a DLE can be forced ahead of any character in the Transmitter Holding Register when CR15 is a logic one in the sync mode.

Bit 5 — In the *Asynchronous* mode a logic 1, with the Transmitter enabled, causes a single Stop bit to be transmitted. A logic 0 causes 2-Stop bit transmission for character lengths of 6, 7, or 8 bits and one-and-a-half Stop bits for a character length of 5 bits.

With the Transmitter disabled this bit controls the Miscellaneous output on Pin 19, which may be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.

In the Synchronous mode a logic 1 combined with a logic 0 on Bit 6 of Control Register 1 enables Transmit parity; if CR15 = 0 or CR15 = 1 no parity is generated. When set to a logic 1 with Bit 6 also a logic 1, the contents of the DLE register are transmitted prior to the next character loaded in the Transmitter Holding Register as part of the Transmit Transparent mode.

Bit 4 — In the *Asynchronous* mode a logic 1 enables the Automatic Echo mode when the receiver section is enabled. In this mode the clocked regenerated data is presented to the Transmit Data output in place of normal transmission through the Transmitter Register. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Only the first character of a Break condition of all zeroes (null character) is echoed when a Line Break condition is detected. For all subsequent null characters, with logic zero Stop bits, a steady Marking condition is transmitted until normal character reception resumes. Echoing does not start until a character has been received and the Transmitter is idle. The Transmitter does not have to be enabled during the Echo mode.

In the *Synchronous* mode a logic 1, with the Receiver enabled, does not allow assembled

Receiver data matching the DLE register contents to be transferred to the Receiver Holding Register; also, parity checking is disabled.

When the Receiver is not enabled this bit controls the Miscellaneous output on Pin 19, which may be used for New Sync on a 201 Data Set. When operating with a 32X clock and a disabled Receiver a logic 1 on this bit also causes the Receiver timing to synchronize on Mark-To-Space transitions.

Bit 3 — In the *Asynchronous* mode a logic 1 enables check of parity on received characters and generation of parity for transmitted characters.

In the *Synchronous* mode a logic 1 bit enables check of parity on received characters only. **Note:** Transmitter parity enable is controlled by CR15.

Bit 2 — A logic 1 enables the ASTRO to receive data into the Receiver Holding Register, update Receiver Status Bits 1, 2, 3, and 4, and to generate Data Received interrupts. A logic 0 disables the Receiver and clears the Receiver Status bits.

Bit 1 — Controls the $\overline{\text{Request To Send}}$ output on Pin 38 to control the CA circuit of the Data Set. The $\overline{\text{RTS}}$ output is inverted from the state of CR11. A logic 1 combined with a low logic $\overline{\text{Clear To Send}}$ input enables the Transmitter and allows THRE interrupts to be generated. A logic 0 disables the Transmitter and turns off the external $\overline{\text{Request To Send}}$ signal. Any character in the Transmitter Register will be completely transmitted before the Transmitter is turned off. The $\overline{\text{Request To Send}}$ output may be used for other functions such as "Make Busy" on 103 Data Sets.

Bit 0 — Controls the $\overline{\text{Data Terminal Ready}}$ output on Pin 16 to control the CD circuit of the Data Set. A logic 1 enables the Carrier and Data Set Ready interrupts. A logic 0 enables only the telephone line Ring interrupt. The $\overline{\text{DTR}}$ output is inverted from the state of CR10.

Control Register 2

Control Register 2, unlike Control Register 1, cannot be changed at any time. This register should be changed only while both the receiver and transmitter sections of the ASTRO are in the idle state.

Bits 7-6— These bits select the character length as follows:

Bits 7-6	Character Length
00	8 bits
01	7 bits
10	6 bits
11	5 bits

When parity is enabled it must be considered as a bit when making character length selection, i.e. 5 character bits plus parity = 6 bits.

Bit 5 — A logic 1 selects the Synchronous Character mode. A logic 0 selects the Asynchronous Character mode.

Bit 4 — A logic 1 selects odd parity and a logic 0 selects even parity, when parity is enabled by CR13 and/or CR15.

Bit 3 — In the *Asynchronous* mode a logic 0 selects the rate 1-32X clock input (pin 30) as the Receiver Clock rate and a logic 1 selects the same clock rate for the Receiver as selected by Bits 2-0 for the Transmitter. This bit must be a logic 1 for the 1X clock selection by Bits 2-0.

In the *Synchronous* mode a logic 1 causes all DLE-SYN combination characters in the Transparent mode when DLE strip CR14 is a logic 1, or all SYN characters in the Non-transparent mode to be stripped and no Data Received interrupt to be generated. The SYN Detect status bit is set with reception of the next assembled character as it is transferred to the Receiver Holding Register.

Bits 2-0 — These bits select the Transmit and Receive clocks. The Input Clock to the Rate 4 pin may be divided down to form the 32X clock from a multiple clock as shown:

Bits 2-0	Clock
000	1X clock for Transmit and Receive (Pins 35 and 34 respectively)
001	32X clock — Rate 1 input (Pin 30)
010	32X clock — Rate 2 input (Pin 31)
011	32X clock — Rate 3 input (Pin 32)
100	32X clock — Rate 4 input ÷ 1 (Pin 33)
101	32X clock — Rate 4 input ÷ 2 (Pin 33)
110	32X clock — Rate 4 input ÷ 4 (Pin 33)
111	32X clock — Rate 4 input ÷ 8 (Pin 33)

BIT 7 6	5	4	3	2 1 0
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS	MODE SELECT 0—ASYNCHRONOUS MODE 1—SYNCHRONOUS MODE	SYNC/ASYNC 1—ODD PARITY SELECT 0—EVEN PARITY SELECT	ASYNC 1—RECEIVER CLOCK DETERMINED BY BITS 2-0 0—RECEIVER CLK = RATE 1 SYNC (CR14 = 0) 0—NO SYN STRIP 1—SYN STRIP SYNC (CR14 = 1) 0—NO DLE-SYN STRIP 1—DLE-SYN STRIP	SYNC/ASYNC CLOCK SELECT 000 - IX CLOCK 001 - RATE 1 CLOCK 010 - RATE 2 CLOCK 011 - RATE 3 CLOCK 100 - RATE 4 CLOCK 101 - RATE 4 CLOCK ÷ 2 110 - RATE 4 CLOCK ÷ 4 111 - RATE 4 CLOCK ÷ 8

CONTROL REGISTER 2

Status Register

The data contained in the Status Register define Receiver and Transmitter data conditions and status of the Data Set. The Status word is shown and defined below.

Bit 7 — This bit is set to a logic 1 whenever there is a change in state of the Data Set Ready or Carrier Detector inputs while Data Terminal Ready (Bit 0 of Control Register 1) is a logic 1 or the Ring Indicator is turned on, with DTR a logic 0. This bit is cleared when the Status Register is read onto the Data Access Lines.

Bit 6 — This bit is the logic complement of the Data Set Ready input on Pin 28. With 202-type Data Sets it can be used for Secondary Receive.

Bit 5 — This bit is the logic complement of the Carrier Detector input on Pin 29.

Bit 4 — In the *Asynchronous* mode a logic 1 indicates that received data contained a log 0 bit after the last data bit of the character in the stop bit slot, while the Receiver was enabled. This indicates a Framing error. This bit is set to a logic 0 if the proper logic 1 condition for the Stop bit was detected.

In the *Synchronous* mode a logic 1 indicates that the contents of the Receiver Register matched the contents of the SYN Register. The condition of this bit remains for a full character assembly time. If SYN strip (CR23) is enabled this status bit is updated with the character received after the SYN character. In both modes the bit is cleared when the Receiver is disabled.

Bit 3 — When the DLE Strip is enabled (Bit 4 of Control Register 1) the Receiver parity check is disabled and this bit is set to a logic 1 if the previous character to the presently assembled character matched the contents of the DLE register; otherwise it is cleared. The DLE DET remains for one character time and is rest on the next character transfer or on a Status Register Read. If DLE Strip is not enabled this bit is set to a logic 1 when the Receiver is enabled, Receiver parity (Bit 3 of Control Register 1) is also enabled, and the last received character has a Parity error. A logic 0 on this bit indicates correct parity. This bit is cleared in either of the above modes when the Receiver is disabled.

Bit 2 — A logic 1 indicates an Overrun error which occurs if the previous character in the Receiver Holding Register has not been read and Data Received is not reset, at the time a new character is to be transferred to the Receiver Holding Register. This bit is cleared when no Overrun condition is detected, i.e., the next character transfer time or when the Receiver is disabled.

Bit 1 — A logic 1 indicates that the Receiver Holding Register is loaded from the Receiver Register, if the Receiver is enabled. It is cleared to a logic 0 when the Receiver Holding Register is read onto the Data Access Lines, or the Receiver is disabled.

Bit 0 — A logic 1 indicates that the Transmitter Holding Register does not contain a character while the Transmitter is enabled. It is set to a logic 1 when the contents of the Transmitter Holding Register is transferred to the Transmitter Register. It is cleared to a 0 bit when the Transmitter Holding Register is loaded from the DAL, or when the Transmitter is disabled.

INPUT/OUTPUT OPERATIONS

All Data, Control, and Status words are transferred over the Data Access Lines (DAL 0-7). Additional input lines provide controls for addressing a particular unit, and regulating all input and output operations. Other lines provide interrupt capability to indicate to a Controller that an input operation is requested by the ASTRO. All input/output terminology below is referenced to the Controller so that a Read or Input takes data from the ASTRO and places it on the DAL lines, while a Write or Output places data from the DAL lines into the ASTRO.

Read

A Read Operation is initiated by the placement of an *eight-bit address* on the DAL by the Controller. When the Chip Select signal goes to a logic low state, the ASTRO compares Bits 7-3 of the DAL with its hard-wired ID code (Pins 17, 22, 24, 25, and 26) and becomes selected on a Match condition. The ASTRO then sets its REPLY line low to acknowledge its readiness to transfer data. Bits 2-0 of the address are used to select ASTRO registers to read from as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	Status Register
110	Receiver Holding Register

When the Read Enable (RE) line is set to a logic low condition by the Controller the ASTRO gates

128	64	32	16	8	4	2	1
BIT 7	6	5	4	3	2	1	0
• DATA SET CHANGE	• DATA SET READY	• CARRIER DETECTOR	• FRAMING ERROR • SYN DETECT	• DLE DETECT • PARITY ERROR	• OVERRUN ERROR	• DATA RECEIVED	• TRANSMITTER HOLDING REGISTER EMPTY

STATUS REGISTER

the contents of the addressed register onto the DAL. The Read operation terminates, and the devices becomes unselected, when both the Chip Select and Read Enable return to a logic high condition. Reading of the Receiver Holding Register clears the DR Status bit. Bit 0 must be a logic low in read or write operations.

Write

A Write operation is initiated by the placement of an eight-bit address or the DAL by the Controller. The ASTRO compares Bits 7-3 of the DAL with its ID code when the $\overline{\text{Chip Select}}$ input goes to a logic low state. If a Match condition exists, the device is selected and makes it $\overline{\text{RPLY}}$ line low to acknowledge its readiness to transfer data. Bits 2-0 of the address are used to select ASTRO registers to be written into as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	SYN and DLE Register
110	Transmitter Holding Register

When the $\overline{\text{Write Enable}}$ ($\overline{\text{WE}}$) line is set to a logic low condition by the Controller the ASTRO gates the data from the DAL into the addressed register. If data is written into the Transmitter Holding Register, the THRE Status bit is cleared to a logic zero.

The 100 address loads both the SYN and DLE registers. After writing into the SYN register the device is conditioned to write into the DLE if followed by another Write pulse with the 100 address. Any intervening Read or Write operation with other addresses resets this condition such that the next 100 will address the SYN register.

Interrupts

The following conditions generate interrupts:

1. **Data Received (DR)** — Indicates transfer of a new character to the Receiver Holding Register while the Receiver is enabled.

2. **Transmitter Holding Register Empty (THRE)** — Indicates that the THR register is empty while the Transmitter is enabled. The first interrupt occurs when the Transmitter becomes enabled if there is an empty THR, or after the character is transferred to the Transmitter Register making the THR empty.

3. **Carrier On** — Indicates Carrier Detector input goes low when DTR is on.

4. **Carrier Off** — Indicates $\overline{\text{Carrier Detector}}$ input goes high when DTR is on.

5. **DSR On** — Indicates the $\overline{\text{Data Set Ready}}$ input goes low when DTR is on.

6. **DSR Off** — Indicates the $\overline{\text{Data Set Ready}}$ input goes high when DTR is on.

7. **Ring On** — Indicates the $\overline{\text{Ring Indicator}}$ input goes low when DTR is off.

Each time an Interrupt condition exists the $\overline{\text{INTR}}$ output from the ASTRO is made a logic low. The following interrupt procedure is then carried out even if the interrupt condition is removed.

The Controller acknowledges the Interrupt request by setting the $\overline{\text{Chip Select}}$ ($\overline{\text{CS}}$) and the $\overline{\text{Interrupt Acknowledge Input}}$ ($\overline{\text{IACKI}}$) to the ASTRO to a Low state. On this transition all non-interrupting devices receiving the $\overline{\text{IACKI}}$ set their $\overline{\text{Interrupt Acknowledge Output}}$ ($\overline{\text{IACKO}}$) low, enabling lower priority daisy-chained devices to respond to the Interrupt request. The highest priority device that is interrupting will then set its $\overline{\text{RPLY}}$ low. This device places its ID code on Bit Positions 7-3 of the DAL when a low $\overline{\text{RE}}$ signal is received. In addition Bit 2 is set to a logic one if any of the interrupt numbers 1 and 3-7 above occurred, and remains a logic low if the THRE has caused the interrupt (see note).

To reset the Interrupt condition ($\overline{\text{INTR}}$) Chip Select ($\overline{\text{CS}}$) and $\overline{\text{IACKI}}$ must be received by the ASTRO. A setup time must exist between $\overline{\text{CS}}$ and the $\overline{\text{RE}}$ or $\overline{\text{WE}}$ signals to allow chip selection prior to read/write operations and deselection control through the latter signals. The data is removed from the DAL when the $\overline{\text{RE}}$ signal returns to the logic high state.

MAXIMUM RATINGS

V_{DD} With Respect to V_{BB} (Ground)		+ 20 to − 0.3V
Max Voltage To Any Input With Respect to V_{BB}		+ 20 to − 0.3V
Operating Temperature		0°C to 70 °C
Storage Temperature	Plastic	-55°C to +125°C
	Ceramic	-65°C to +150°C
Power Dissipation		1000 mW

NOTE:
The UC1671-1 places Data Received on $\overline{\text{DAL1}}$ and THRE on $\overline{\text{DAL0}}$ during interrupt servicing. The UC1671-0 places the $\overline{\text{DAL1}}$ and $\overline{\text{DAL0}}$ into a Three State Mode during interrupt.

OPERATING CHARACTERISTICS

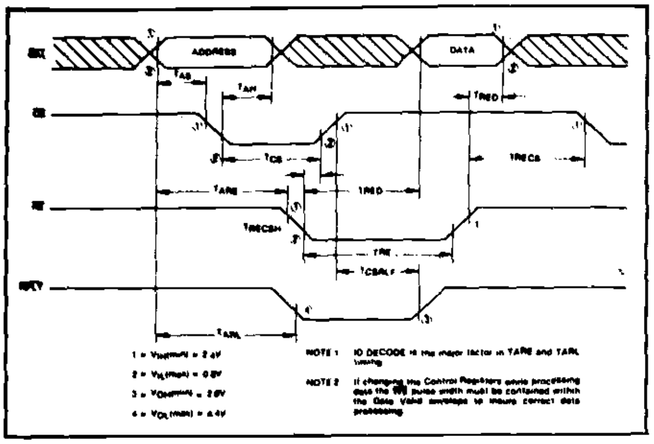
T_A = 0°C to 70 °C, V_{DD} = +12.0V ± .6V, V_{BB} = −5.0 ± .25V, V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{DD}$
I_{BB}	V_{BB} Supply Current			1	mA	$V_{BB} = -5V$
I_{CCAVE}	V_{CC} Supply Current			80	mA	
I_{DDAVE}	V_{DD} Supply Current			10	mA	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage (All Inputs)			.8	V	
V_{OH}	Output High Voltage	2.8			V	$I_O = -100\,\mu A$
V_{OL}	Output Low Voltage			.4	V	$I_O = 1.6\,mA$

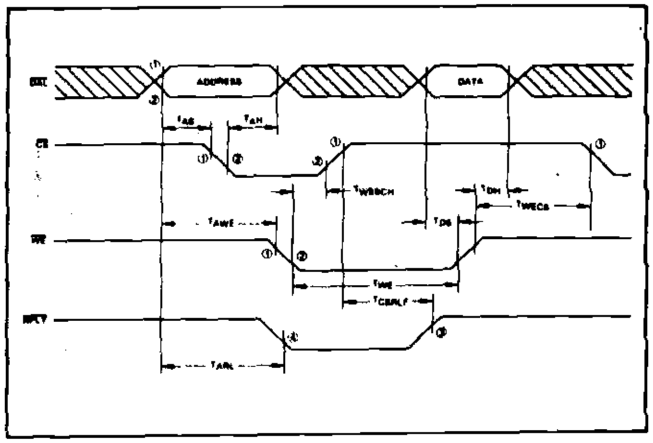
AC CHARACTERISTICS

T_A = 0°C to 70 °C, V_{DD} = +12.0V ± 0.6V, V_{BB} = −5.0V ± 0.25V, V_{CC} = +5.0 ± .25V, V_{SS} = 0V
CL_{MAX} = 20 pf

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{AS}	Address Set-Up Time	0			ns	
t_{ah}	Address Hold Time	150			ns	
T_{ARL}	Address to $\overline{RPLY}$ Delay			400	ns	
T_{CS}	$\overline{CS}$ Width	250			ns	
T_{CSRLF}	$\overline{CS}$ to Reply OFF Delay	0		250	ns	$R_L = 2.7\,K\Omega$
READ						
T_{ARE}	Address and $\overline{RE}$ Spacing	250			ns	
T_{RECSH}	$\overline{RE}$ and $\overline{CS}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{RED}	$\overline{RE}$ to Data Out Delay			180	ns	$C_L = 20\,pf$
T_{RE}	$\overline{RE}$ Width	200		1000	ns	
WRITE						
T_{AWE}	Address to $\overline{WE}$ Spacing	250			ns	
T_{WECSH}	$\overline{WE}$ and $\overline{CS}$ Overlap	20			ns	
T_{WE}	$\overline{WE}$ Width	200		1000	ns	
T_{DS}	Data Set-Up Time	150			ns	
T_{DH}	Data Hold Time	100			ns	
T_{WECS}	$\overline{WE}$ to $\overline{CS}$ Spacing	250			ns	



READ CYCLE TIMING DIAGRAM

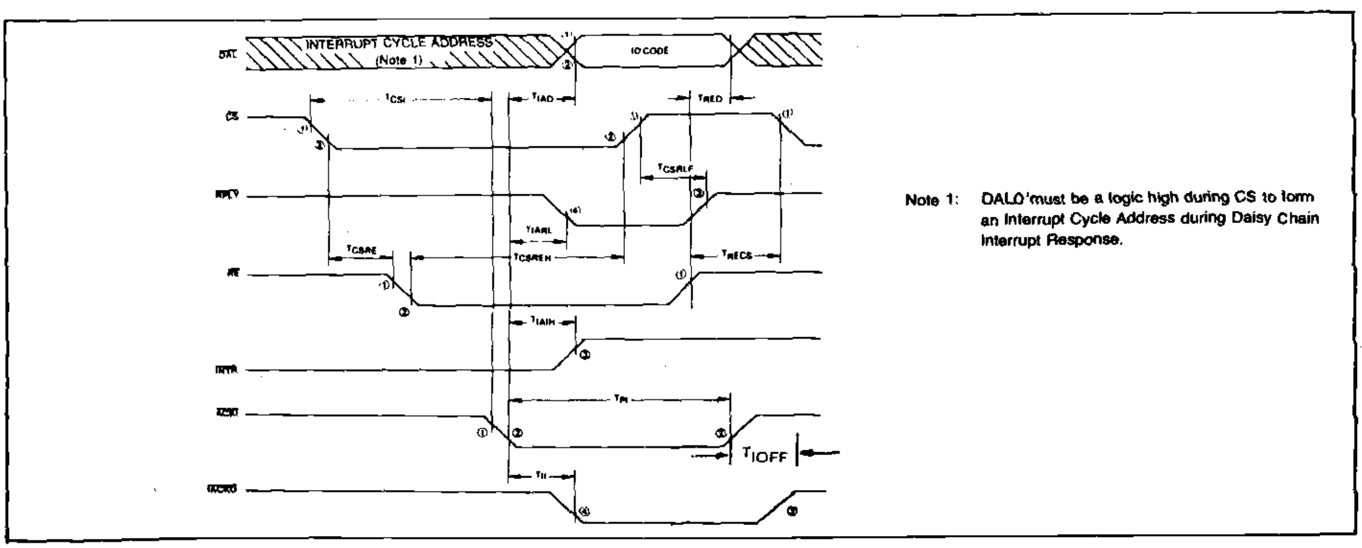


WRITE CYCLE TIMING DIAGRAM

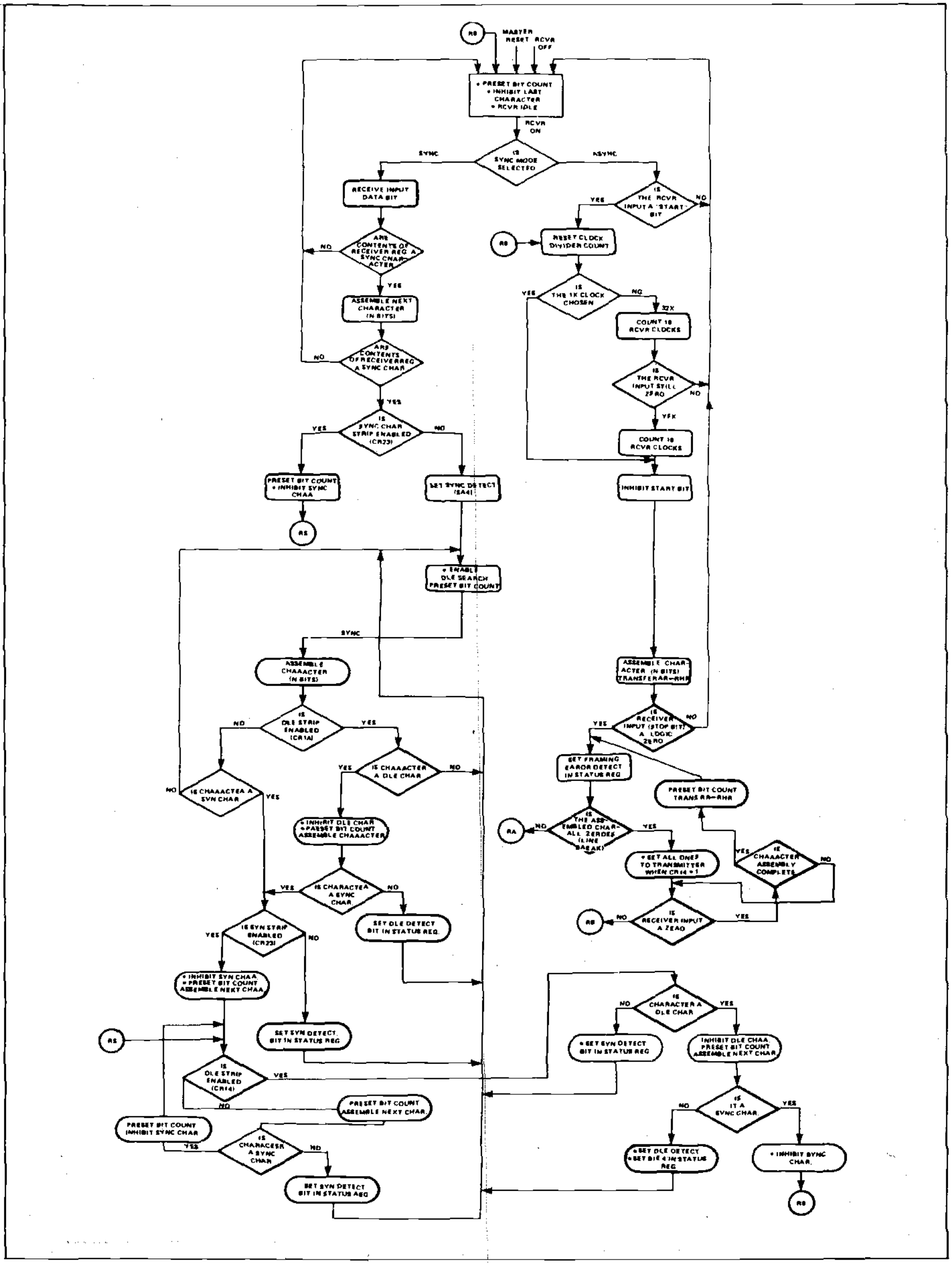
INTERRUPT

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{CSI}	$\overline{CS}$ to $\overline{IACKI}$ Delay	0			ns	
T_{CSRE}	$\overline{CS}$ to $\overline{RE}$ Delay	250			ns	
T_{CSREH}	$\overline{CS}$ and $\overline{RE}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{PI}	$\overline{IACKI}$ Pulse Width	200			ns	
T_{IAD}	$\overline{IACKI}$ to Valid ID Code Delay			250	ns	See Note 1.
T_{RED}	$\overline{RE}$ OFF to $\overline{DAL}$ Open Delay			180	ns	
T_{IARL}	$\overline{IACKI}$ to $\overline{RPLY}$ Delay			250	ns	
T_{CSRLF}	$\overline{CS}$ to $\overline{RPLY}$ OFF Delay	0		250	ns	R_L = 2.7 KΩ
T_{IAIH}	$\overline{IACKI}$ ON to $\overline{INTR}$ OFF Delay			300	ns	
T_{II}	$\overline{IACKI}$ to $\overline{IACKO}$ Delay			200	ns	
T_{IOFF}	$\overline{IACKO}$ OFF Delay From $\overline{CS}$ OFF, RE OFF, or $\overline{IACKI}$ HIGH.			250	ns	See Note 2.

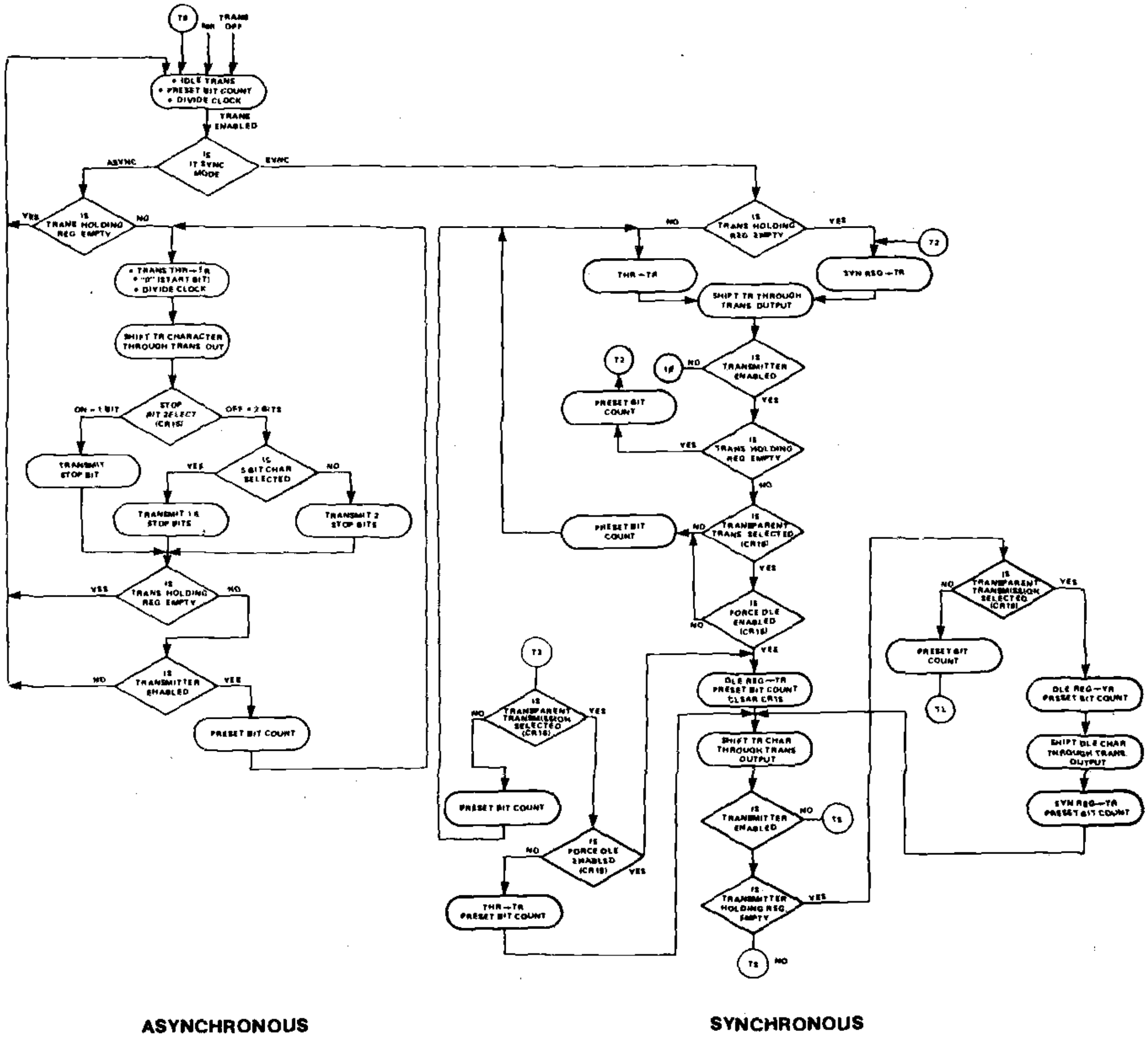
Note 1: If $\overline{RE}$ goes low after $\overline{IACKI}$ goes low, the delay will be from the falling edge of $\overline{RE}$.
Note 2: $\overline{IACKO}$ goes false after the last one of the following three signals go false: $\overline{CS}$, $\overline{RE}$ and $\overline{IACKI}$. T_{IOFF} is measured from the last signal going false.



INTERRUPT CYCLE TIMING DIAGRAM



RECEIVER SECTION



TRANSMITTER SECTION